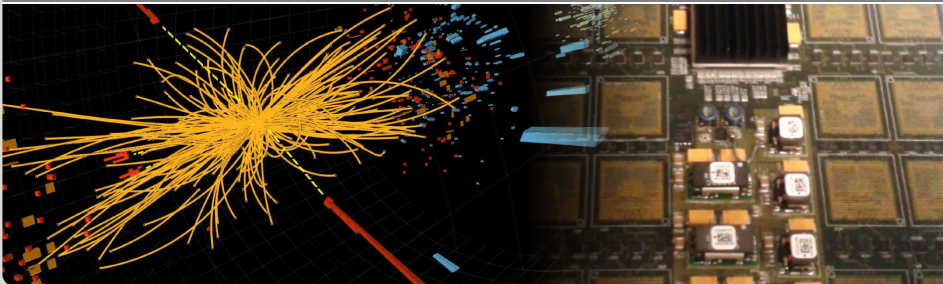


# The CMS Track Trigger and the Processing of its Data

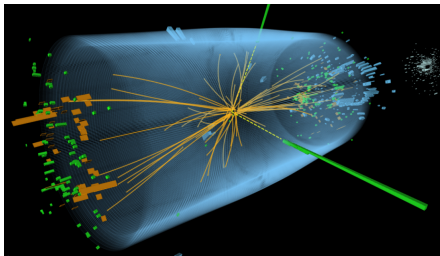
Christian Amstutz

Institute for Data Processing and Electronics (IPE)

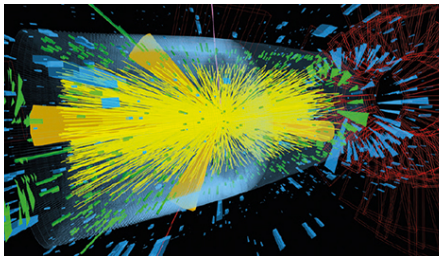


# So many Particles!

Recorded Event (2012)

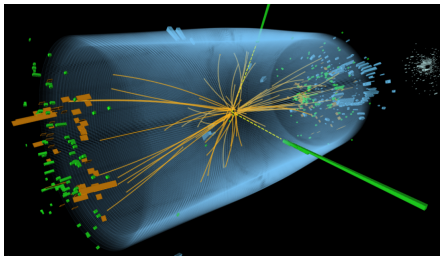


Simulation for HL-LHC (2025)

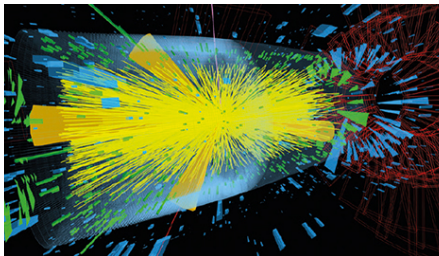


# So many Particles!

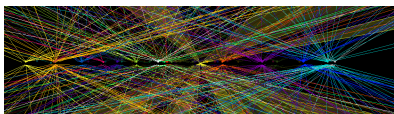
Recorded Event (2012)



Simulation for HL-LHC (2025)



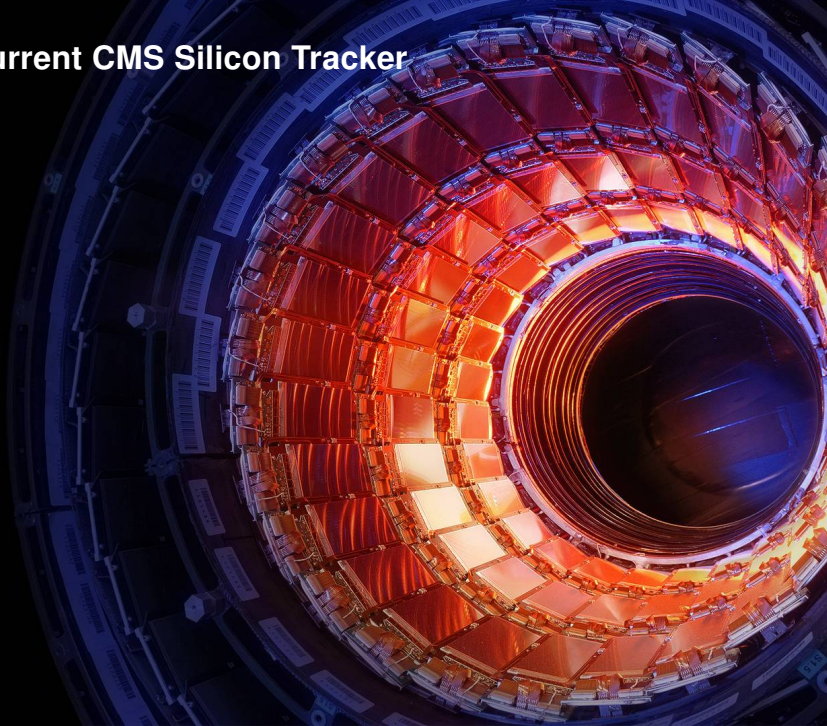
$\approx 10$  cm



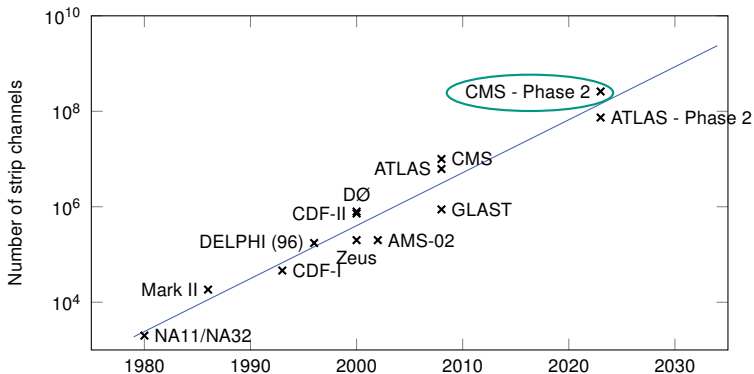
## High-Luminosity LHC:

- Concurrent Collisions: up to 200
- Number Tracks:  $\approx 10000$

# The Current CMS Silicon Tracker



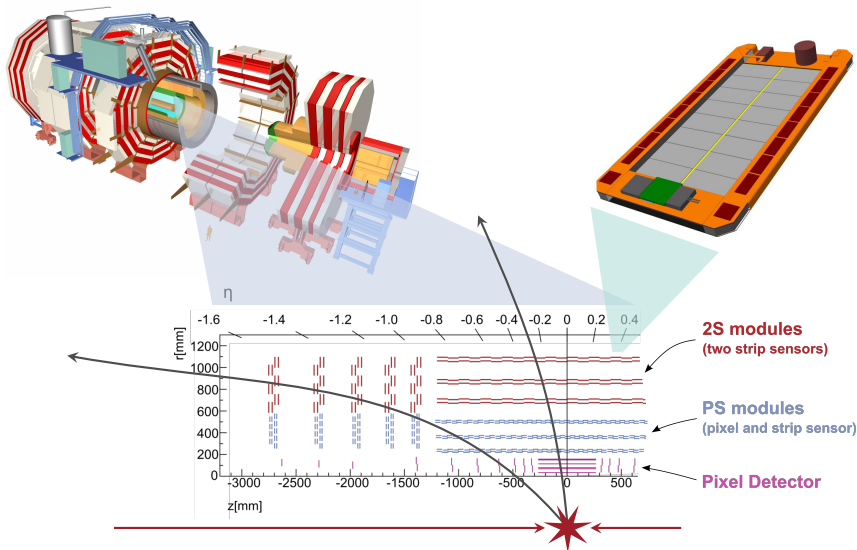
# Evolution of Channels in Silicon Trackers



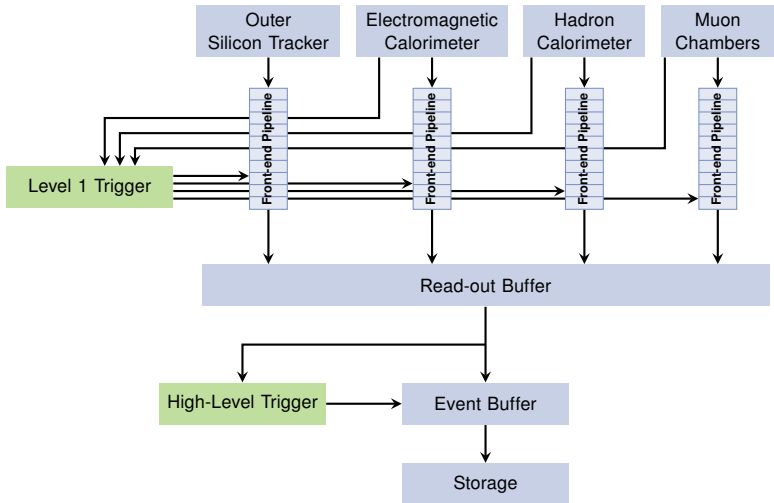
Silicon detectors: **1.7** times more channels every two years

Moore's law: **2** times more transistors every two years

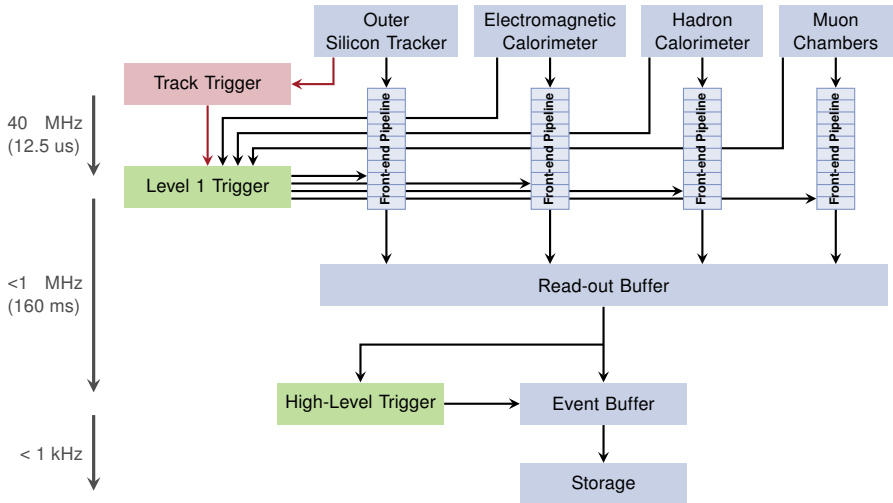
# The CMS Silicon Tracker for HL-LHC



# The Trigger System of CMS – *today*



# The Trigger System of CMS – at the *HL-LHC*





# Challenges of the CMS Track Trigger

Bunch collision rate:	<b>40 MHz</b>
Data rate produced by the detector:	<b>11'200 Tbit/s</b>
Data rate transmitted to Track Trigger:	<b>50 Tbit/s</b>
Optical Fibers:	<b>15000</b>
Latency (Sensor - L1 Trigger - Sensor):	<b>&lt; 12.5 us</b>

**Goal:** Providing High-Energy Tracks to the Level-1 Trigger.

# An Approach using Associative Memories (AM)

Working principle of Content Addressable Memories (CAM):

Christian Amstutz

# An Approach using Associative Memories (AM)

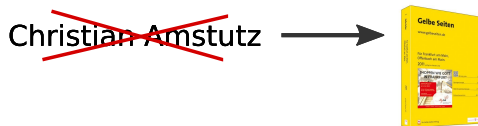
Working principle of Content Addressable Memories (CAM):

Christian Amstutz



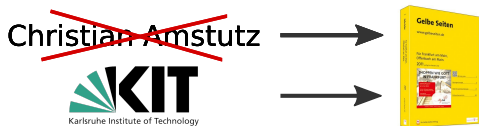
# An Approach using Associative Memories (AM)

Working principle of Content Addressable Memories (CAM):



# An Approach using Associative Memories (AM)

Working principle of Content Addressable Memories (CAM):



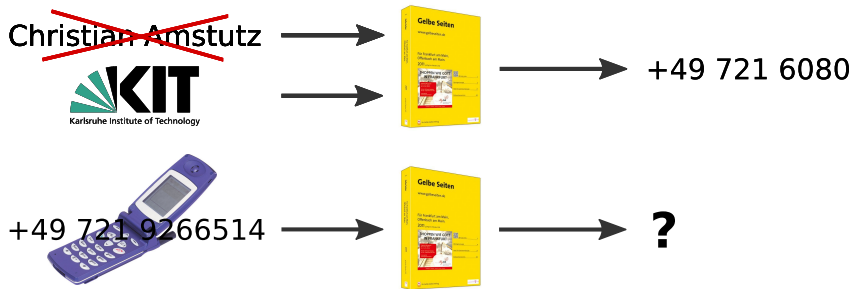
# An Approach using Associative Memories (AM)

Working principle of Content Addressable Memories (CAM):



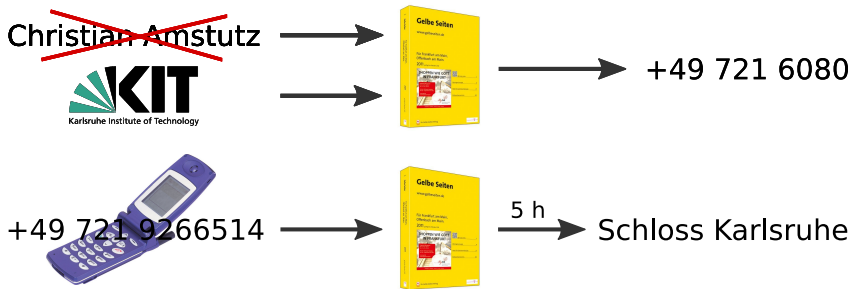
# An Approach using Associative Memories (AM)

Working principle of Content Addressable Memories (CAM):



# An Approach using Associative Memories (AM)

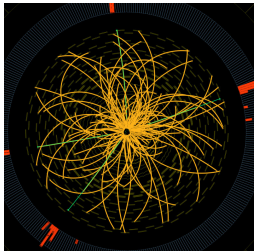
Working principle of Content Addressable Memories (CAM):



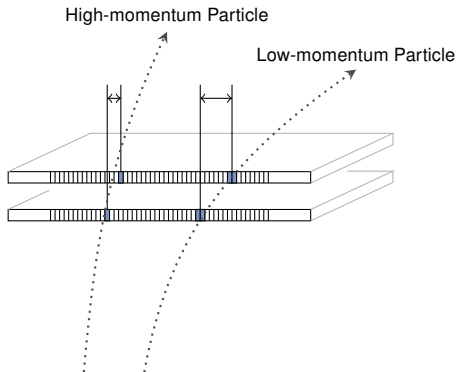
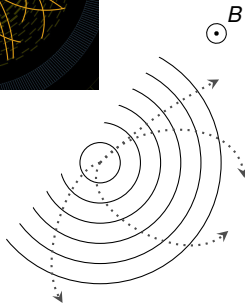
▶ Very fast lookup whether content is available



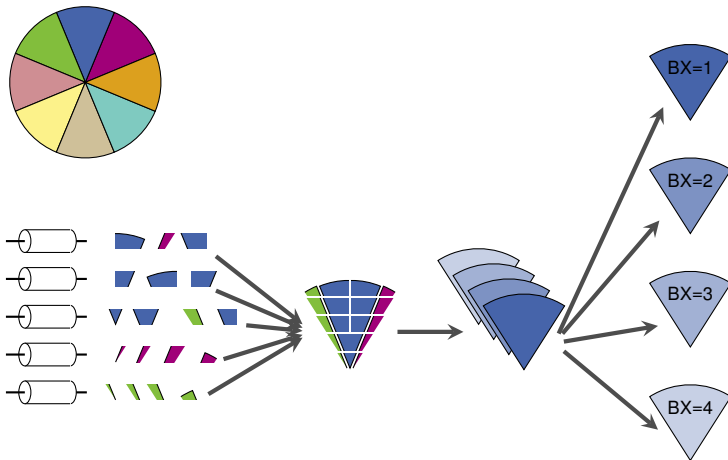
# Stacked Modules and Stubs



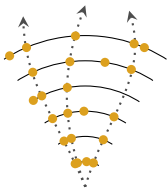
Accepted particles:  $p_T > 3 \text{ GeV}$



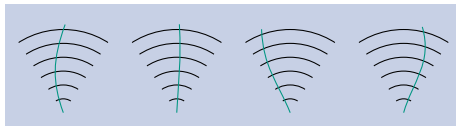
# Arranging the Tracker Data



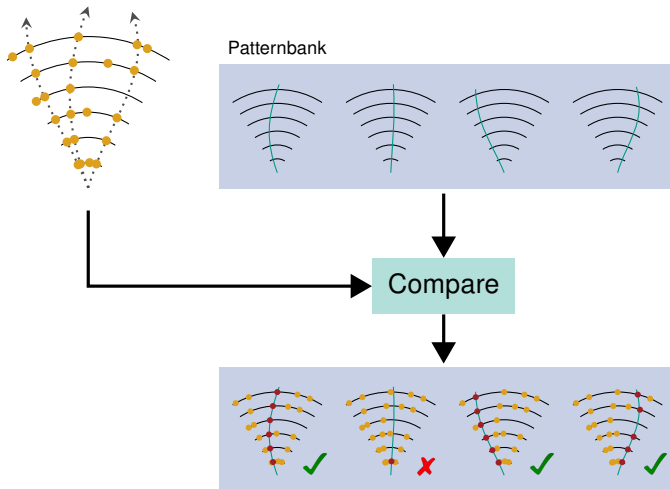
# Track Finding by Associative Memory



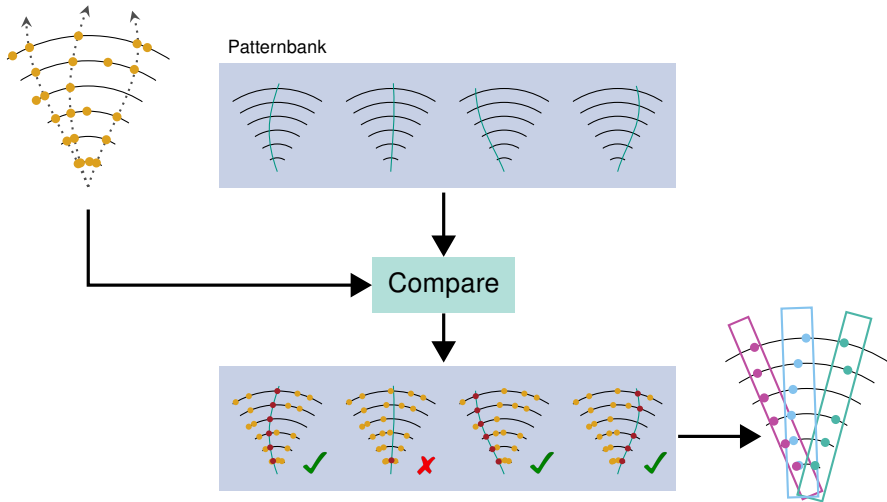
Patternbank

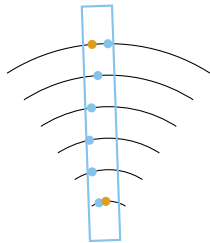


# Track Finding by Associative Memory

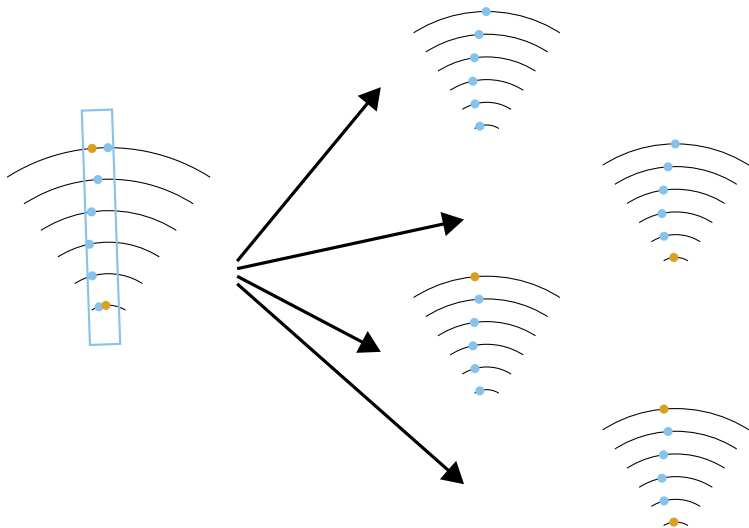


# Track Finding by Associative Memory

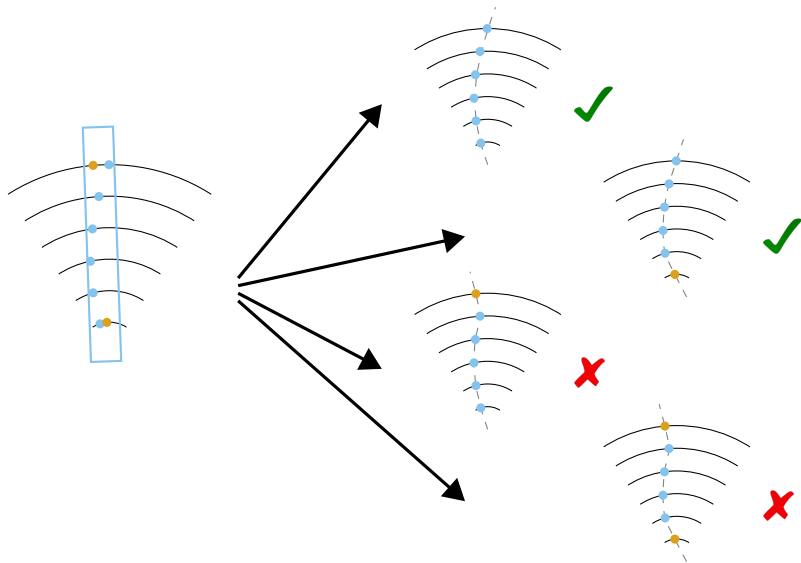




# Event Building

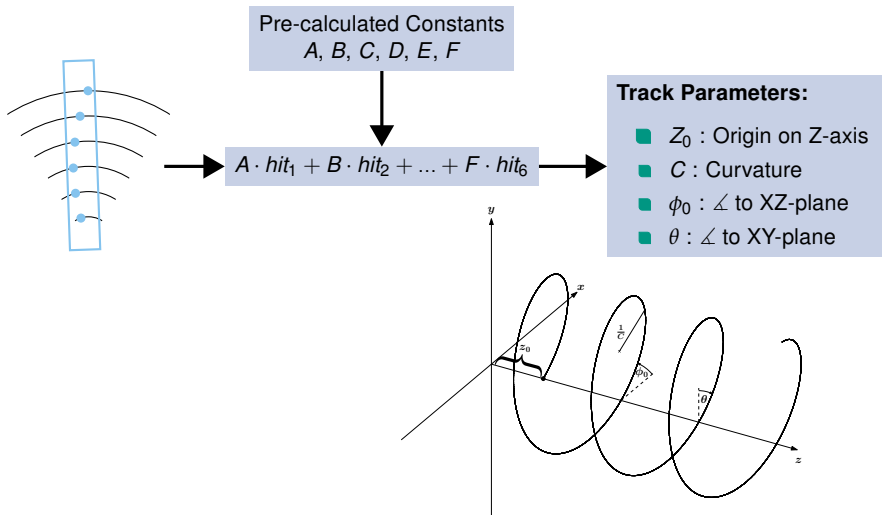


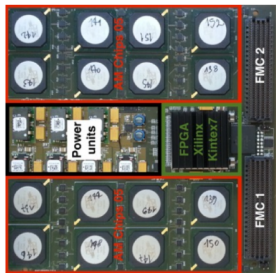
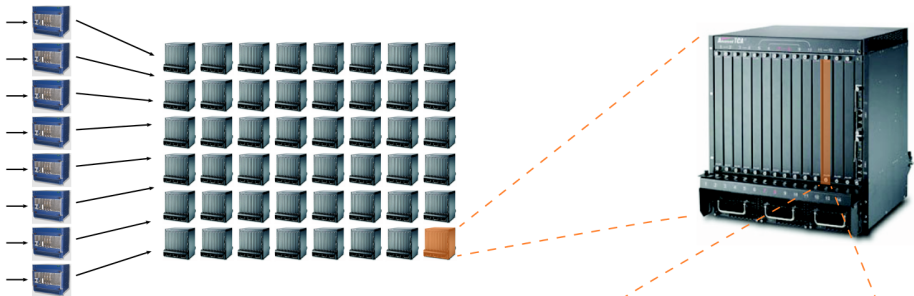
# Event Building





# Track Fitting by Linearized Fit





**Idea:** Model an essential part of the CMS Track Trigger electronics

## Goals:

- Evaluation of system properties (latencies, link bandwidths, ...)
- Evaluation of system architectures
- Generation of test vectors for hardware debugging

## Realization

- Realized in SystemC (a C++ library)
- All existing modules, but not all details
- Parameters of modules configurable



**Idea:** Model an essential part of the CMS Track Trigger electronics

## Goals:

- Evaluation of system properties (latencies, link bandwidths, ...)
- Evaluation of system architectures
- Generation of test vectors for hardware debugging

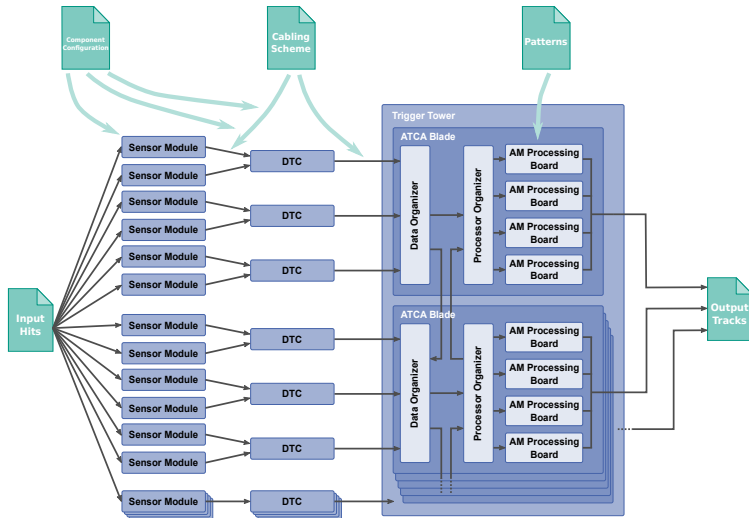
## Realization

- Realized in SystemC (a C++ library)
- All existing modules, but not all details
- Parameters of modules configurable



**One sector of the Track Trigger has been simulated**

# System Simulation II



# FPGA — Programmable Digital Chips

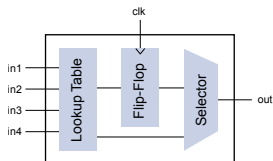
... a very very brief introduction

## Field-Programmable Gate Array

# FPGA — Programmable Digital Chips

... a very very brief introduction

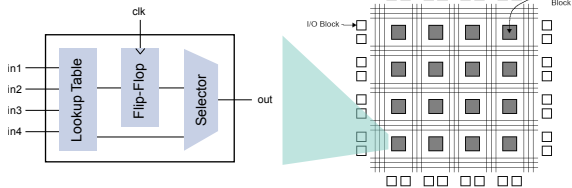
## Field-Programmable Gate Array



# FPGA — Programmable Digital Chips

... a very very brief introduction

## Field-Programmable Gate Array

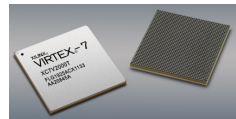
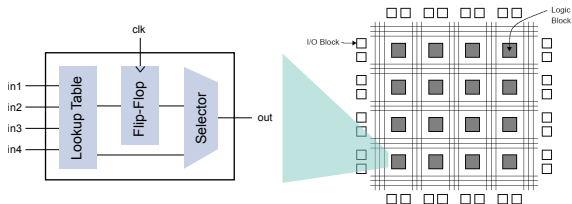




# FPGA — Programmable Digital Chips

... a very very brief introduction

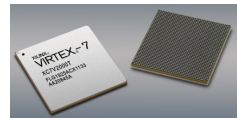
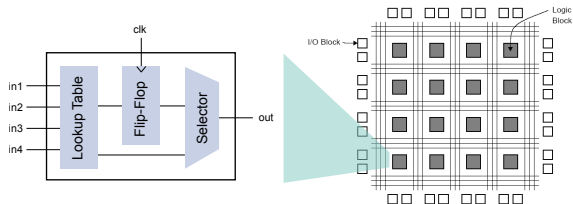
## Field-Programmable Gate Array



# FPGA — Programmable Digital Chips

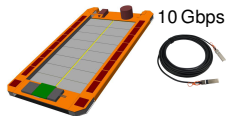
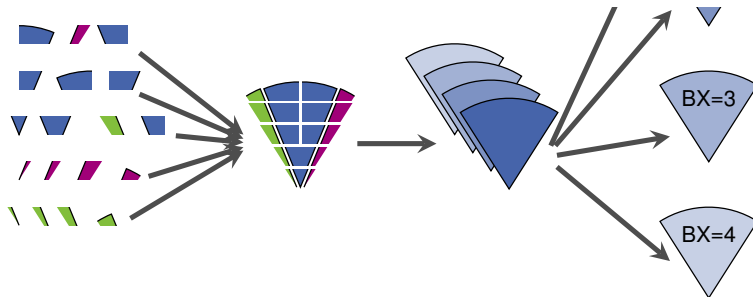
... a very very brief introduction

## Field-Programmable Gate Array



```
multiply_vectors(a[1000], b[1000])  
  for i = 1 to 1000  
    c[i] = a[i] * b[i]  
  return c
```

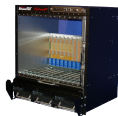
# Electronic System behind the Data Processing



Sensor Module  
15000



MTCA crate  
72



ATCA crate  
48

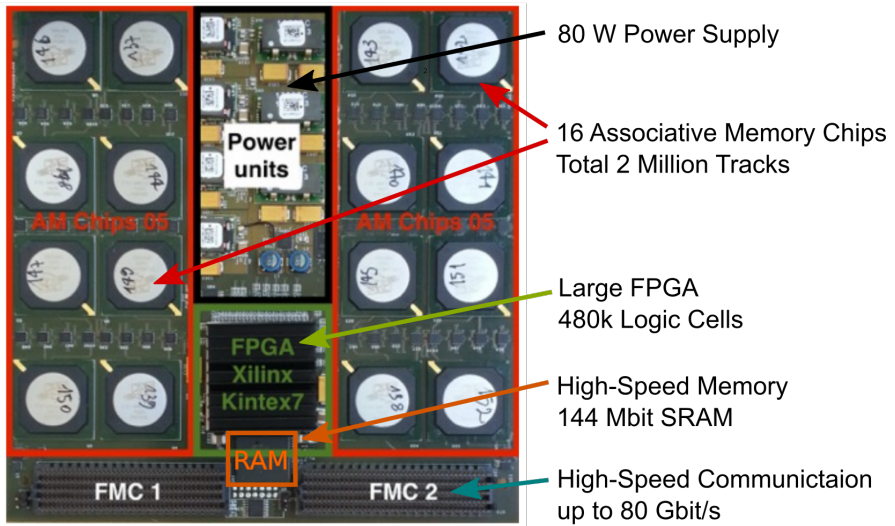


Pulsar-IIb Board  
550



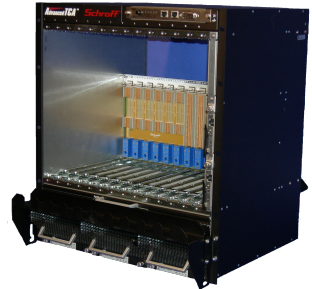
AM Board  
2200

# The Pattern Recognition Mezzanine



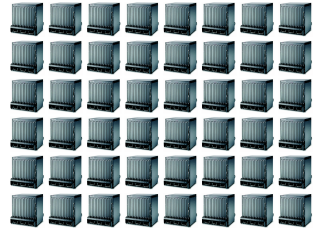
# Cost Estimation for the Track Trigger

1	ATCA crate	8k €
	Cables and transceivers	24k €
12	<i>ATCA blades:</i>	
12	Printed Circuit Boards	36k €
12	FPGAs	64k €
12	AM Chip sets	64k €
<hr/>		
		<b>196k €</b>



# Cost Estimation for the Track Trigger

1	ATCA crate	8k €
	Cables and transceivers	24k €
12	<i>ATCA blades:</i>	
12	Printed Circuit Boards	36k €
12	FPGAs	64k €
12	AM Chip sets	64k €
<hr/>		
		<b>196k €</b>



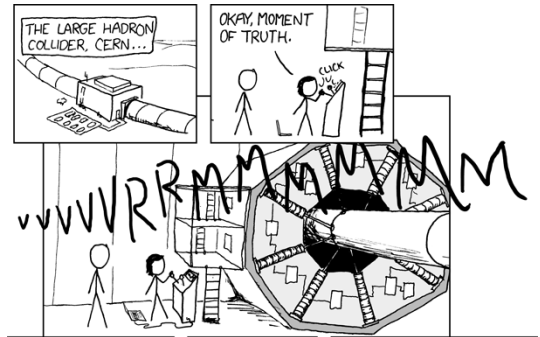
Total equipment cost: 48 crates \* 196k € = **9.4M €**

# Conclusion

- One of the most complex electronic systems ever built
- Contributions of many groups are necessary
- Very competitive spirit between different groups

 **The Track Trigger is essential for CMS HL-LHC**

# Thank you for your attention



source: [www.xkcd.com](http://www.xkcd.com)