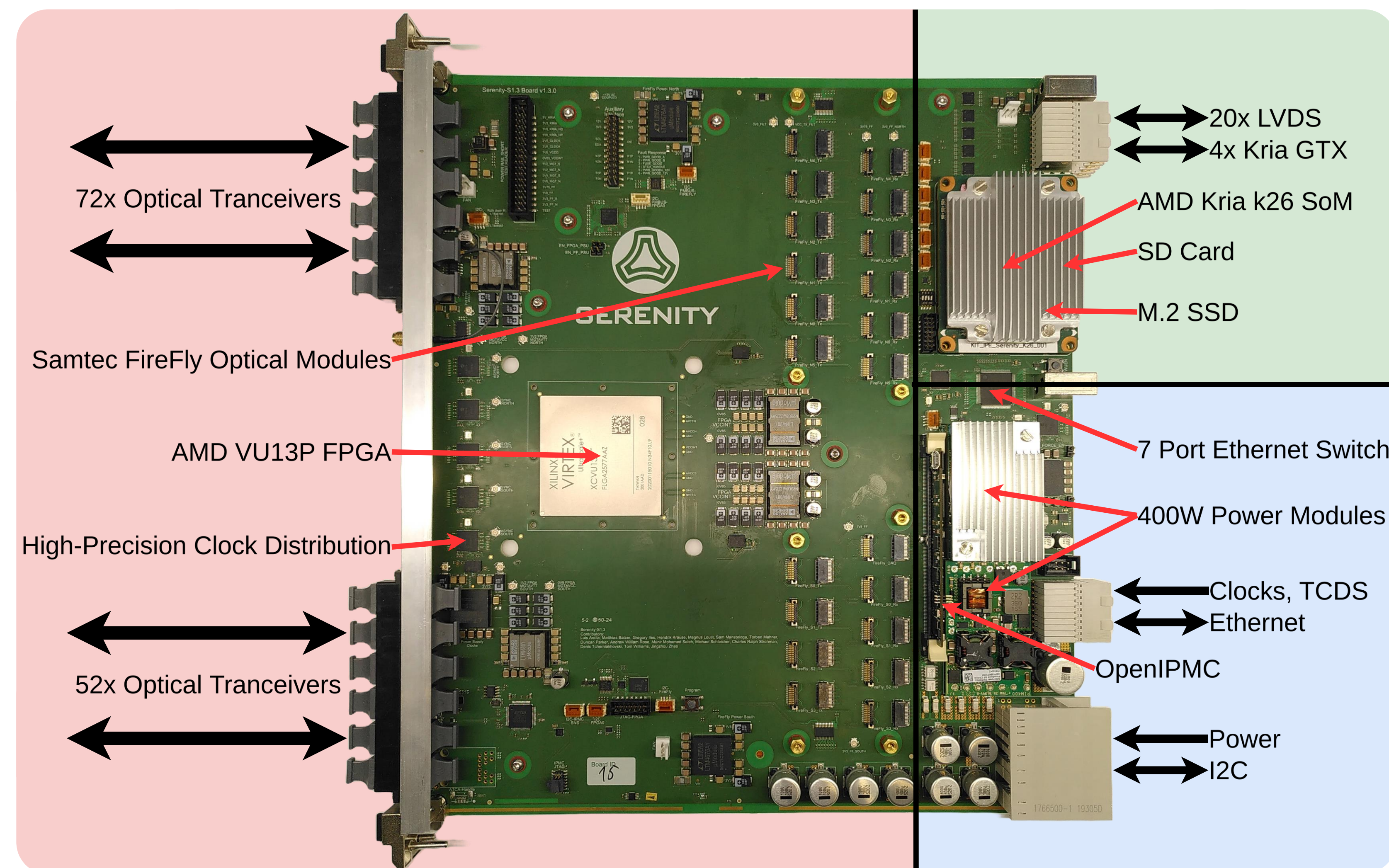


Serenity-S1: A Versatile Data Processing Board for CMS Phase-2

H. Krause, L. Ardila-Perez, M. Balzer, M. Fuchs and T. Mehner on behalf of the Serenity consortium
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Payload Area

- Performance optimized
- Two FPGA options
 - AMD **VU13P** or VU9P
- Multiple FireFly options
 - 10x T12 / R12, 1x B04
 - Copper / optical
 - Up to **25 Gb/s**
- Sync or async clock paths
- Central power control

Service Area

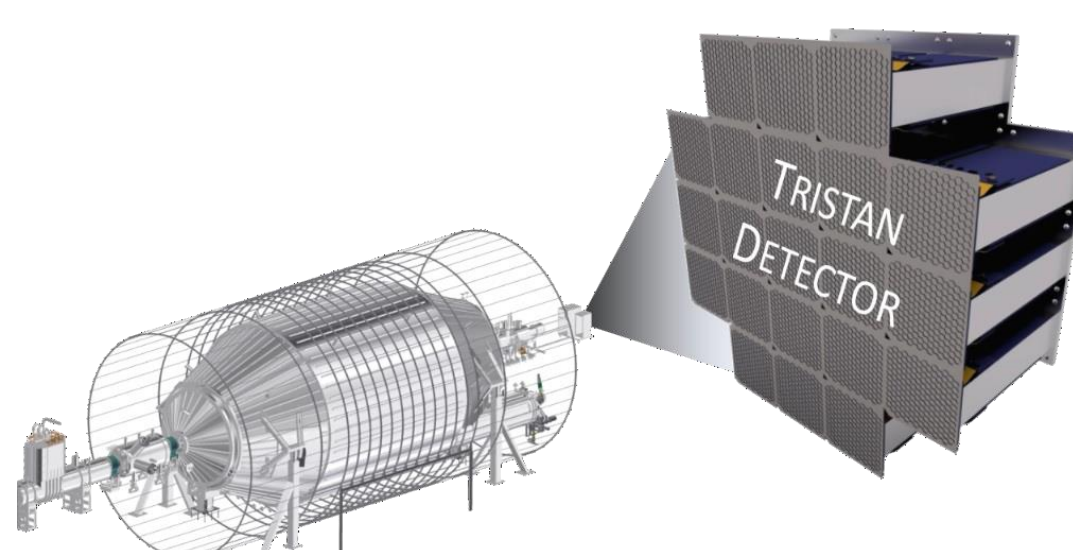
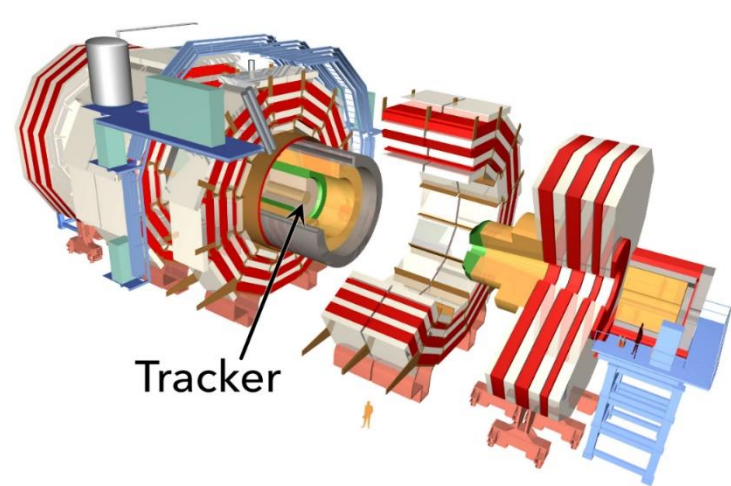
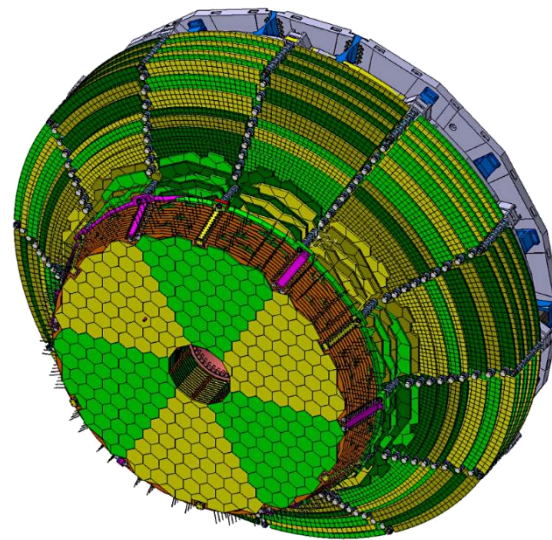
- Space optimized
- Board management
- AMD **Kria k26 SoM**
 - ARM CPU + FPGA
 - Splitboot network boot

ATCA Infrastructure

- Space optimized
- Monitoring and control per ATCA standard
 - OpenIPMC**
- Cascade power modules

Versatile Applications

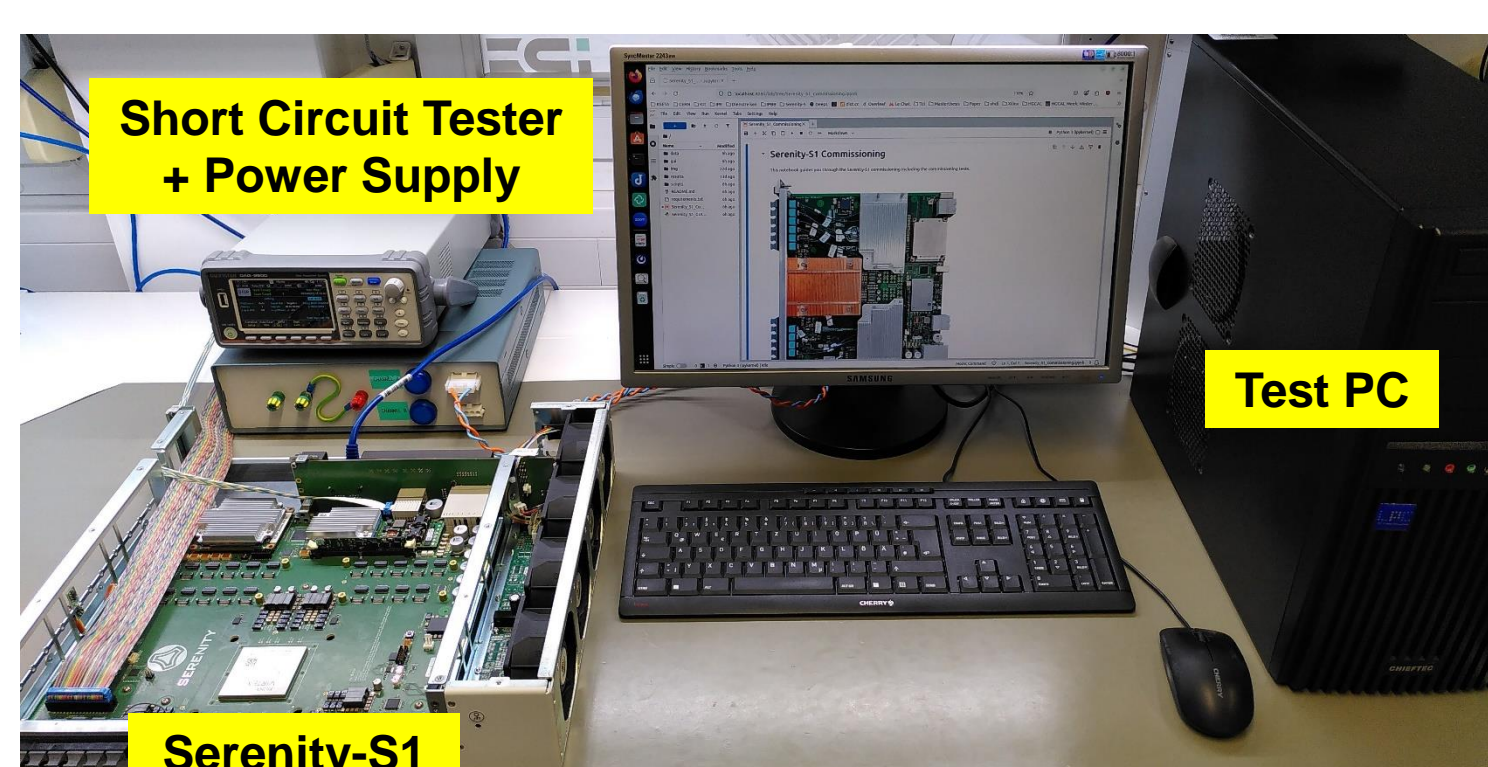
- The High-Granularity-Calorimeter (**HGCAL**) will replace the endcap calorimeters in CMS
- Due to high data rates, **302 Serenity-S1 cards** will be used for DAQ and trigger
- CMS Tracker** will be upgraded for HL-LHC
- 214 Serenity-S1 cards** will be used as DAQ and timing cards (DTC)
- 104 additional Serenity-S1 cards** will be used by various other CMS subsystems for phase-2 (**BRIL, MTD, L1T, ...**)
- TRISTAN** is the next experiment generation at KATRIN
- New detector requires new readout system with online cluster-evaluation
- 3 Serenity-S1 cards** will be used



➔ **Suitable for large- and small-scale setups!**

Road to Production and Testing

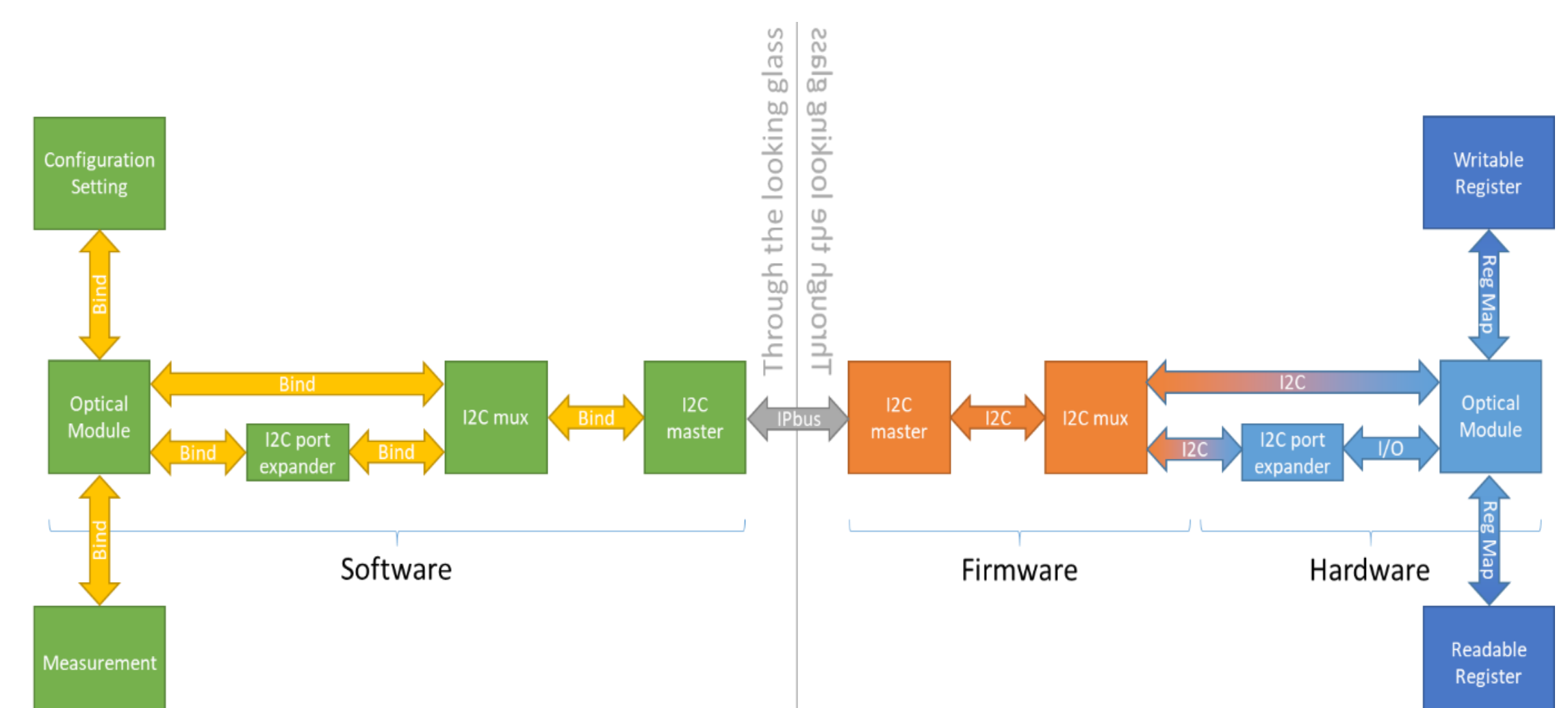
- Pilot** started in **April 2024** (10x S1.2 cards)
- Extended Pilot** started in **November 2024** (18x S1.3 cards)
- Pre-Production** starts in **April 2025** (84x S1.4 cards)
- Production** starts in **December 2025** (638x S1.4 cards)
- ➔ **Hardware development almost done!**
- Factory Acceptance Test**
 - Test / Configure every board in **10 Minutes**
 - Highly automated
- User Acceptance Test**
 - Sub-detector specific tests at CERN
- ➔ **My work ensures every board is properly tested!**



Advanced Board Management

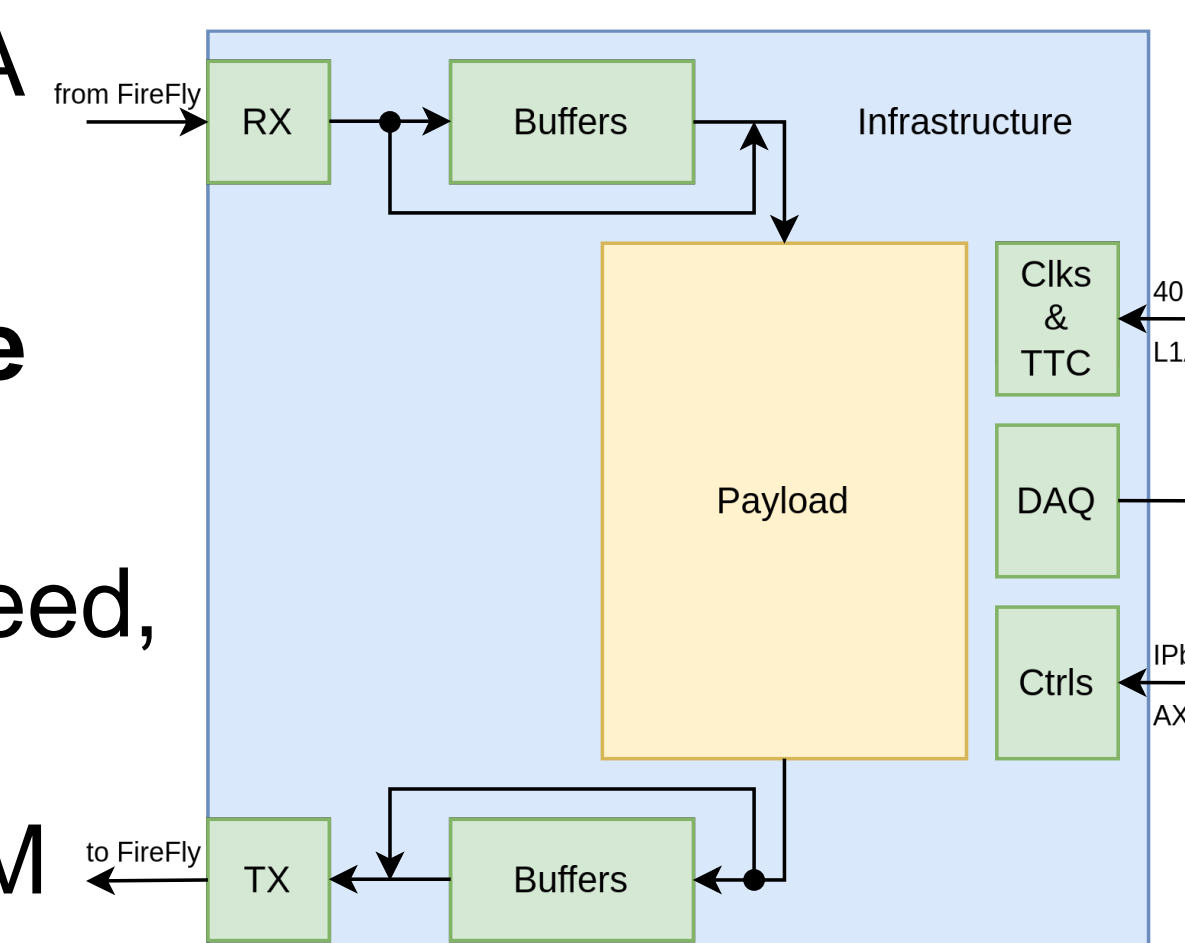
Serenity Management Shell (SMASH)

- Framework that runs on the Kria k26 SoM
- Controls the board communication infrastructure
 - I2C** and **PMBus** based
- Works by mirroring the physical bus topology into software
- Flexible** against **hardware changes** through independent modules connected by bind commands



Extensible Modular (data) Processor (EMP)-Framework

- Framework that runs on the FPGA
- Centered around a **payload area**
- Infrastructure **easily configurable** via single config file
 - Link Type/Protocol, Clock Speed, Buffer, ...
- Register access from the Kria SoM
 - IPBus** via AXI chip2chip



➔ **You can focus on your awesome physics algorithm!**

Interested and want to know more?!
Visit our Webpage for more information about the board and tools



Trust me, it is not a rick roll