KSETA-Working Report 2016

"Real-time high-performance readout system (100 Tb/s) for the CMS track trigger High Energy Physics detectors"

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1 Introduction

At the CMS experiment each bunch crossing produces on the order of 10,000 stubs (pairs of hits in a double side detector). Only about 5 to 10% of these stubs actually belong to primary tracks with pT $>$ 2 GeV (approximately 125 particles collision per bunch crossing). The rest are random combinations of hits, or are due to lower-pT particles and secondary particles produced by interactions of primary particles with the material in the detector. The goal of the L1 track finding system is to perform pattern recognition to reconstruct the tracks of primary particles with pT $>$ 2 GeV, and discard as many as possible of all the other stubs.
The Time Multiplex Track Trigger (TMTT) approach for the CMS L1 track trigger is composed of various stages, namely: 1) track finding, 2) track fitting and 3) duplicate track removal. The first stage is composed by the Geometric Processor (GP) which subdivides the octant into sectors and the Hough Transform (HT) which performs a simple tracking in the r/ϕ plane. The second stage contains the Track Filter/Fitter (TF) which cleans tracks and fits their helix parameters. Finally the third stage, the Duplicate Removal (DR) eliminates those tracks which got accidentally reconstructed multiple times by the first two stages, refer to Figure 1.

2 Progress on Doctorate

The TMTT approach for the CMS L1 Track Trigger is highly modular and each processing stage can be developed independently from the others guaranteeing developer independence and the possibility of designing different variations on certain particular stages. The first months of my doctorate I spent familiarizing myself with the already designed stages and analyzing the possibility of implementing them on an heterogeneous system. At KIT the UFO framework was developed as a flexible data acquisition system capable of taking and analyzing

data in real-time. Necessary optimizations were made in the communication between system components to guarantee the low-latency behavior required by the CMS L1 track trigger. This work led to several publications and conference presentations in which is shown how near-future GPU and FPGA technology could allow the implementation of such a complex and demanding system with off-the-shelf parts.

After September due to the collaborative nature of the project, I have been located at the Rutherford Appleton Laboratory in the United Kingdom where I took responsibility of implementing in firmware (VHDL) algorithms designed in C++ for the third and last processing stage, the duplicate removal. Several duplicate removal architectures and designs were explored in terms of resource usage, processing latency, complexity and tracking efficiency. The final choice was made to select the design which was the simplest, using the least resources but still providing a very good tracking efficiency. The tracking efficiency for the entire processing chain is about 94.5 % for a TTBar + 200 Pile-Up event.

A great effort was put into designing the firmware in such a way that it would use the least FPGA resources and in the most efficient way only occupying about 0.20 % LUT, 0.18 % LUTRAM, 0.34 % FF and 0.81 % BRAM for processing the entire 36 sectors in a detector octant. Two 32×64 matrices used in an interleaved way every event log the position of the tracks in the hough space per sector, using the information from the track finding and track fitting stages it is possible to determine whether a track is a duplicate or not. The chosen algorithm is capable of identify duplicates by only looking at a singular track, not having the need of comparing against other tracks allows for a massive simplification and FPGA resource savings. Only tracks which have the same hough space bin after both stages are consider true tracks, and those which are unique in a particular hough space bin are allowed in a second phase of the algorithm.

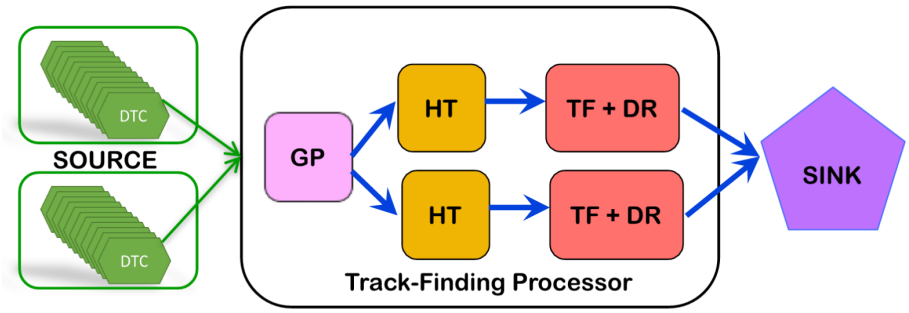

Figure 1: TMTT Hardware Demonstrator Architecture Dec 2016 Review

The firmware describing the above algorithm was completed for the Phase 2 CMS L1 Tracking review carried out on December at CERN. The duplicate removal firmware was used as part of the hardware demonstrator presented by the TMTT group. A total of 8 MP7 boards in a μTCA crate were used.

The duplicate removal thanks to its light weight was integrated along with the kalman filter/fitter in the same MP7 board as shown in the Figure 1, each box in the Figure corresponds to an MP7 board. A publication presenting the current hardware and software developments is on preparation.

3 Publications

Articles

[1] M. Caselle, L.E. Ardila Perez, M. Balzer, A. Kopmann, L. Rota, M. Weber, M.Brosi, J. Steinmann, E. Bründermann, and A.-S. Müller. "KAPTURE-2. A picosecond sampling system for individual THz pulses with high repetition rate". In: *Journal of Instrumentation* 12.01 (2017), p. C01040. URL: http://stacks.iop.org/1748-0221/12/i=01/a=C01040.

[2] L. Rota, M. Vogelgesang, L.E. Ardila Perez, M. Caselle, S. Chilingaryan, T. Dritschler, N. Zilio, A. Kopmann, M. Balzer, and M. Weber. "A high-throughput readout architecture based on PCI-Express Gen3 and DirectGMA technology". In: *Journal of Instrumentation* 11.02 (2016), P02007. URL: http://stacks.iop.org/1748-0221/11/i=02/a=P02007.

Posters and Proceedings

[3] M. Caselle, L. Ardila Perez, S. Chilingaryan, T. Dritschler, A. Kopmann, H. Mohr, L. Rota, M. Vogelgesang, M. Balzer, and M. Weber. "High-speed low-latency readout system with realtime trigger based on GPUs". In: *Real Time Conference*. June 2016. URL: https://indico.cern.ch/event/390748/contributions/1825218/attachments/1281568/1917838/Trigger2_99_Caselle.pdf.

[4] M. Caselle, L. Ardila Perez, L. Rota, A. Kopmann, H. Mohr, S. Chilingaryan, T. Dritschler, M. Vogelgesang, M. Balzer, and M. Weber. "A High-Speed DAQ Framework for Future High-Level Trigger and Event Building Clusters". In: *TWEEP2016*. 2016. URL: http://indico.cern.ch/event/489996/contributions/2213195/.

[5] H. Mohr, L. Ardila Perez, M. Balzer, M. Caselle, L. Rota, A. Kopmann, H. Mohr, S. Chilingaryan, T. Dritschler, M. Vogelgesang, and M. Weber. "Evaluation of GPUs for High-Level Triggers in High Energy Physics". In: *TWEEP2016*. 2016. URL: http://indico.cern.ch/event/489996/contributions/2211076/.

[6] M. Vogelgesang, L. Rota, L.E. Ardila Perez, M. Caselle, S. Chilingaryan, and A. Kopmann. "High-throughput data acquisition and processing for real-time x-ray imaging". In: vol. 9967. 2016. DOI: 10.1117/12.2237611. URL: http://dx.doi.org/10.1117/12.2237611.