KSETA-Working Report 2017

"Real-time high-performance readout system (100 Tb/s) for the CMS track trigger High Energy Physics detectors"

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1 Introduction - An FPGA based track finding architecture

A new tracking detector is under development for use by the CMS experiment at the High-Luminosity LHC (HL-LHC). A crucial requirement of this upgrade is to provide the ability to reconstruct all charged particle tracks with transverse momentum above 2 GeV within 4 μs so they can be used in the Level-1 trigger decision.
It is proposed to divide the tracker into eight 45 degree φ-sectors, each rotated by approximately 22.5 degrees in φ with respect to the detector octant boundaries, so that each DTC (Data, Trigger and Control) handles data belonging to no more than two neighboring processing octants, the DTC is responsible for converting front-end link data to a global coordinate system and to perform time multiplexing to 18 output nodes (Figure 1).

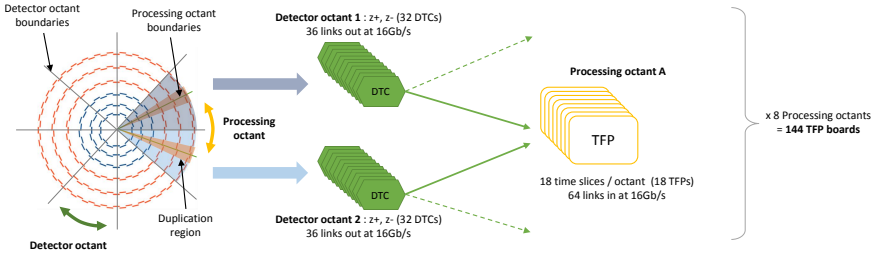

Figure 1: Baseline system architecture with 18 time nodes and eight processing octants. The full track finding system would be composed of 144 Track Finding Processors (TFPs).

The Track Finding Processor (TFP) is composed by the following stages, refer to Figure 2:
1) Geometric Processor (GP) - responsible for processing the stub data and subdividing the octant into finer sub-sectors in η and φ to simplify the track finding task and to increase parallelization;
2) Hough Transform (HT) - a highly parallelized first stage track finder that identifies groups of stubs that are coarsely consistent with a track hypothesis in the r-φ plane, so reducing combinatorics in the downstream steps;
3) Kalman Filter (KF) - a second stage candidate cleaning and precision fitting algorithm to remove fake tracks and improve helix parameter resolution;
4) Duplicate Removal (DR) - final pass filter using the precise fit information to remove any duplicate tracks generated by the Hough Transform.

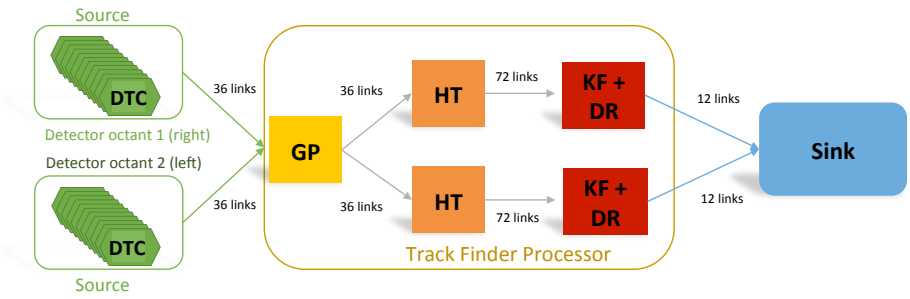

Figure 2: TMTT Hardware Demonstrator Architecture Dec 2016 Review, each box inside the Track-Finding Processor corresponds to an MP7 FPGA board

2 Progress on Doctorate - Optimization of the Geometric Processor

Each GP pre-processes the 48-bit DTC stubs from one processing octant, both unpacking the data into a 64-bit extended format to reduce processing load on the HT, and assigning the stubs to geometric sub-sectors, which are angular divisions of the octant. The GP firmware consists of a pre-processing block, which calculates the correct sub-sector for each stub based on its global coordinate position, followed by a layered routing block. The stubs associated to each sub-sector are routed to dedicated outputs, such that data from each sub-sector can be processed by an independent HT array.
As depicted in Figure 3, the GP subdivides its processing octant into 36 sub-sectors, loosely referred to as (η, φ) sub-sectors, formed from two divisions in the r-φ plane and 18 divisions in the r-z plane. The division of the octant into sub-sectors simplifies the task of the downstream logic, so that track finding can be carried out independently and in parallel within each of the sub-sectors. The use of relatively narrow sub-sectors in η has the added advantage that it ensures

that any track found by the HT stage must be approximately consistent with a straight line in the r-z plane, despite the fact that the HT itself only does track finding in the r-φ plane.

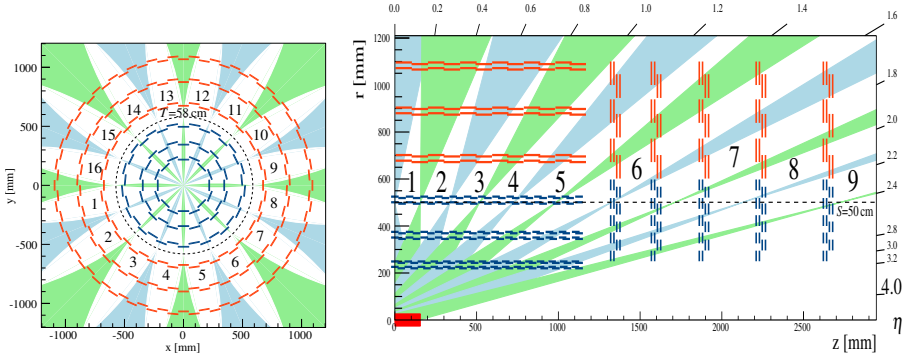

Figure 3: The segmentation of the tracker volume into φ sub-sectors (left) and η sub-sectors (right). The numbered areas in white represent the regions that are associated to only one sector, whereas the colored areas represent the overlap region between neighboring sectors where stubs may need to be assigned to both sectors.

The GP pre-processing block initially written in the high level synthesis language MaxJ was successfully written in VHDL with improved performance and better matching with the corresponding C++ emulation code, 99.88% instead of 99.83%. The better performance helped correctly match about 1000 tracks more in only 100 events, therefore indicating the significance of the 0.05% improvement in the performance. The VHDL module in comparison with the MaxJ implementation utilizes 30% less DSPs and requires as well 48% less number of clock cycles to determine the corresponding sub-sector of a stub.
The different stages of the TFP were implemented in Virtex7 FPGAs for the December 2016 review process, however it is foreseen to use newer FPGA technologies, namely Ultrascale and Ultrascale+ FPGAs, therefore the algorithms used in the GP and other stages are in a process of technological migration so that they could be mapped and optimized specifically for those newer architectures. The GP pre-processing module has been successfully ran at clock frequencies up to 500 MHz in an Ultrascale FPGA. Further improvement includes the modification of the data format from the DTC to include higher granularity in the r and z variables and the modification of the algorithm so that the tilted detector module configuration is supported.

3 Publications

Articles

[1] R. Aggleton, L.E. Ardila-Perez, F.A. Ball, M.N. Balzer, G. Boudoul, J. Brooke, M. Caselle, L. Calligaris, D. Cieri, E. Clement, S. Dutta, G. Hall, K. Harder, P.R. Hobson, G.M. Iles, T.O. James, K. Manolopoulos, T. Matsushita, A.D. Morton, D. Newbold, S. Paramesvaran, M. Pesaresi, N. Pozzobon, I.D. Reid, A.W. Rose, O. Sander, C. Shepherd-Themistocleous, A. Shtipliyski, T. Schuh, L. Skinnari, S.P. Summers, A. Tapper, A. Thea, I. Tomalin, K. Uchida, P. Vichoudis, S. Viret, and M. Weber. "An FPGA based track finder for the L1 trigger of the CMS experiment at the High Luminosity LHC". In: *Journal of Instrumentation* 12.12 (2017), P12019. URL: http://stacks.iop.org/1748-0221/12/i=12/a=P12019.

[2] M. Caselle, L.E. Ardila-Perez, M. Balzer, A. Kopmann, L. Rota, M. Weber, M.Brosi, J. Steinmann, E. Bründermann, and A.-S. Müller. "KAPTURE-2. A picosecond sampling system for individual THz pulses with high repetition rate". In: *Journal of Instrumentation* 12.01 (2017), p. C01040. URL: http://stacks.iop.org/1748-0221/12/i=01/a=C01040.

Posters and Proceedings

[3] L. Ardila-Perez. "TMTT Duplicate Tracks Removal". In: *8th INFIERI Workshop at Fermilab*. Oct. 2016. URL: https://indico.cern.ch/event/557734/contributions/2322836/attachments/1358139/2053961/TMTT_Duplicate_Track_Removal.pdf.

[4] L. Ardila-Perez, F. Ball, M. Balzer, M. Caselle, L. Calligaris, D. Cieri, E. Clement, K. Harder, G. Iles, T. James, K. Manolopoulos, A. Morton, D. Newbold, M. Pesaresi, I. Reid, A. Rose, O. Sander, C. Shepherd-Themistocleous, T. Schuh, S. Summers, I. Tomalin, and M. Weber. "Scalability of the Time Multiplexed CMS Level1 Track Trigger System". In: *4th Summer School on INtelligent signal processing for FrontIEr Research and Industry (INFIERI)*. Jan. 2017. URL: https://indico.cern.ch/event/566138/contributions/2466071/attachments/1407084/2153161/2017_INFIERI_SP_LA.compressed.pdf.