KSETA-Working Report 2018

"Real-time high-performance readout system (100 Tb/s) for the CMS track trigger High Energy Physics detectors"

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January 28, 2019

1 Introduction - The Phase-2 Tracker Back-End Electronics

In the back-end system, track reconstruction is performed using a time-multiplexed architecture requiring two layers of data processing. The first layer, the Data, Trigger, and Control (DTC), extracts and pre-processes the stub data and routes it to the Track Finding layer. Routing of stubs follows a set of rules aimed at splitting the data as a function of time and geometrical origin in the detector. The second layer, the Track Finding Processor (TFP), receives all data for a given event and reconstructs the trajectories of charged particles in the tracker.

Two hardware platforms are being developed as part of the R&D programme currently underway within the level-1 trigger community [1]. One of them called "Apollo" uses a single large FPGA with up to 96 optical links with speeds up to 16 and 25 Gb/s, where Samtec Firefly modules are used for the optical connections. Prototypes will carry at least two mezzanines: an IPMI controller and an embedded Linux endpoint, both based on the Xilinx Zynq 7 series devices. Another approach called "Serenity" [2] envisions two processing sites where different FPGAs can be mounted using a Samtec Z-Ray interposer interconnect. Both processing sites support up to 96 links at 28 Gb/s, using Samtec Firefly optical modules as well. The slow control CPU is a commercial COM-Express Type-10 module with an Intel Atom CPU. The IPMC hardware is supplied by

[1] C. Collaboration, The Phase-2 Upgrade of the CMS L1 Trigger Interim Technical Design Report, Tech. Rep. CERN-LHCC-2017-013. CMS-TDR-017, CERN, Geneva, Sep, 2017.

[2] A. Rose and G. Iles, Serenity - An ATCA prototyping platform for CMS Phase-2, in TWEPP 2018 Topical Workshop on Electronics for Particle Physics, 2018.

CERN running commercial software [3].

2 Progress on Doctorate

2.1 Designing a Processing Daughtercard for Serenity

With the inclusion of two processing sites in Serenity and the use of Z-Ray interposer technology by Samtec it is possible to have different types of configurations, daisy chained, parallel, or parallel with shared bus. For the tracker specific configurations, one could use it to construct two different configurations so that each corresponds to one of the two processing layers required for the time-multiplexed track reconstruction algorithm.

The interconnection needed for the DTC was implemented in a daughtercard featuring the biggest Xilinx Kintex Ultrascale Plus device (KU15P). Each daughtercard is capable of reading the data from up to 36 front-end modules via optical links at 5 or 10 Gb/s. The daughtercard is also connected to the Track Finder via 24 fiber optical links running at 25 Gb/s. The design of the daughtercard was done in a symmetric manner so that two of them could be placed in parallel in one motherboard and be able to send data to one another via the bridge interconnection via the Serenity motherboard.

(a) Bottom layer showing the Samtec Z-Ray footprint.

(b) Top layer with Xilinx KU15P FPGA mounted.

Figure 1: The Serenity KU15P Daughtercard.

[3] J. Mendez, V. Bobillier, S. Haas, M. Joos, S. Mico and F. Vasey, Design of an advancedTCA board management controller (ipmc), Journal of Instrumentation 12 (2017) C03010.

2.1.1 High-Speed Differential Lines Tuning

The high-speed differential lines connecting the gigabit transceivers running at 25 Gb/s were tuned and de-skewed down to less than 100 μm of difference between the positive and negative trace. The corners were rounded and compensation jogs were added to every differential pair to balance the corners in the routing path. A second version of the daughtercard is to be fabricated in the following months including the above optimizations.

2.1.2 High-Speed Optical Transceiver Qualification

A deeper evaluation of optical transceivers is underway with the goal of qualifying quantitatively the capabilities of different optical transceivers from different vendors. FPGA Mezzanine Cards (FMC) are being fabricated mounting different optical components from Samtec, Finisar and Avago with the goal of selecting the best performing component and guarantee that all of them could be interchangeable or transparent for the final system. An FMC board was designed containing one Finisar BOA transceiver with 12 channels TX-RX at 25 Gb/s. Bit Error Rate (BER) tests will be performed using Development FPGA boards currently available with 25 Gb/s transceivers such as the VCU118 from Xilinx.

2.2 Unified Slow Control for the Back-End Electronics System

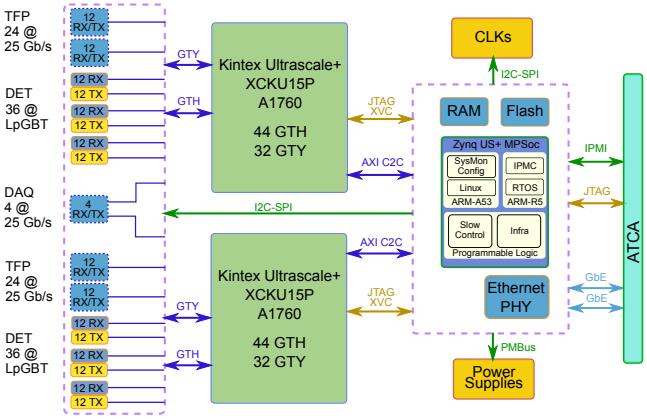


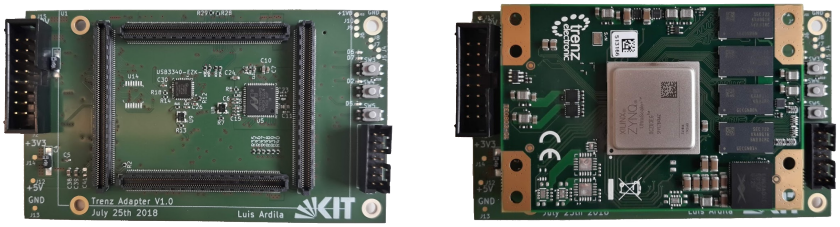
Figure 2: The Ultraflex block diagram.

Ultraflex, new ATCA board in addition to the previously mentioned, explores the idea of using a highly integrated solution for board management and slow

control. It carries a Xilinx Zynq US+ heterogeneous System-on-Chip (SoC) which provides FPGA logic, high-performance ARM-A53 multi-core processors and two ARM-R5 real-time capable processors. The ARM-R5 cores are used to implement time-critical and deterministic tasks using freeRTOS or bare-metal applications. They provide the Intelligent Platform Management Controller (IPMC) functionality and communicate via the backplane of the ATCA crate with the shelf manager, to negotiate the card power-up and subsequent stable operation. The ARM-R5 are also connected to the power supplies (via PMBus), to voltage and current monitors, to clock generators and jitter cleaners (via I2C, SPI) providing the required configuration at start-up. Once full power is enabled from the crate, a Yocto based Linux operating system starts on the powerful ARM-A53 cores. For slow control, the SoC is the central entry point to the two Kintex US+ FPGAs, providing Ethernet interfaces for TCP/IP protocols, IPBus and the like. The communication between the Zynq US+ SoC and the Kintex US+ FPGAs uses the AXI chip-to-chip protocol via LVDS lines or high-speed transceivers.

2.2.1 Trenz-Serenity Adapter

With the aim of validating some of the proposed features of the Ultraflex board in the shortest possible time, an adapter to the Serenity board was designed mapping the COM-Express and CERN-IPMC pins to a commercially available Zynq Ultrascale+ module manufactured by Trenz, featuring the XCZU4EG device [4].



(a) Top layer of the adapter showing the Trenz adapter footprint and some of the physical interface chips.

(b) Zynq US+ Trenz module mounted on the adapter.

Figure 3: The adapter assembly has the footprint of the COM-Express computer-on-module and plugs on the site reserved for it on the Serenity board.

The adapter provides slow control links to the main FPGAs via the Processing System (PS) PCIe link, Programmable Logic (PL) AXI Chip to Chip, and the PL PCIe interface. Direct evaluation and comparison between different slow

[4] Trenz Electronic GmbH, TE0803 - Zynq UltraScale+, 2018.

control approaches is possible. The IPMC application can be verified via its redundant dual connection to the backplane. The configuration of the power supplies and clock synthesizers placed on the motherboard is accessible as well via the adapter. Finally, communication interfaces like Ethernet and USB are supported via onboard physical interface chips.

3 Publications

Articles

[1] L.E. Ardila-Perez. "Level-1 track finding with an all-FPGA system at CMS for the HL-LHC". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2018). ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2018.10.174. URL: http://www.sciencedirect.com/science/article/pii/S0168900218314888.

Posters and Proceedings

[2] A. Akira Shinoda and L.E. Ardila-Perez and L. Arruda Ramalho and M. Balzer and D. Bormann and L. Calligaris and A. Cascadan and V. Finotti and A. França Queiroz da Costa and O. Sander and M. Schleicher and T. Schuh and D. Tcherniakhovski and S. de Souza and M. Weber. "Ultraflex: An ATCA prototype board for the CMS Phase 2 Tracker Upgrade". In: *TWEEP2018*. 2018. URL: https://indico.cern.ch/event/697988/contributions/3056081/attachments/1718840/2773929/poster_TWEPP_ZYNQ.pdf.

[3] L.E. Ardila-Perez. "Duplicate Removal Algorithm of the Time-Multipled Track Trigger of CMS". In: *CMS Phase II Tracker Backend SysDev Workshop*. 2018. URL: https://indico.cern.ch/event/689620/contributions/2879964/attachments/1599315/2534971/DR_2008_02_13.pdf.

[4] L.E. Ardila-Perez. "Level-1 track fining with an all-FPGA system at CMS for the HL-LHC". In: *4th Matter and Technology Helmholtz Meeting*. 2018. URL: https://indico.desy.de/indico/event/19924/session/4/contribution/8/material/slides/0.pdf.

[5] L.E. Ardila-Perez. "The HL-LHC CMS Level-1 Track Trigger". In: *4th Matter and Technology Helmholtz Student Retreat*. 2018. URL: https://indico.desy.de/indico/event/19924/session/4/contribution/8/material/slides/1.pdf.