KSETA-Working Report 2019

"Real-time high-performance readout system (100 Tb/s) for the CMS track trigger High Energy Physics detectors"

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1 Introduction - The Phase-2 Tracker Back-End Slow Control

Data acquisition systems (DAQ) for high energy physics experiments utilize complex FPGAs to handle unprecedented high data rates, this is especially true in the first stages of the processing chain; the CMS tracker back-end electronics performs track reconstruction in under 4 μs. The CMS Tracker DAQ system is arranged in two hardware layers, the first layer reads the detector front-end and performs region sorting and time multiplexing, the second layer performs track reconstruction for a given sector and a particular event, both layers add up to about 500 ATCA-sized boards.

Developing and commissioning these systems becomes more complex as more processing intelligence is placed closer to the detector, in a distributed way directly on the ATCA blades, in the other hand, sophisticated slow control is as well desirable. Reducing the number of intelligent devices is a way of simplify the board design and the interaction between them. Several prototypes contain small FPGA parts, micro-controllers, and SoCs to perform specific tasks which could all be integrated in a single heterogeneous device like the Zynq Ultrascale+ from Xilinx[1].

[1] Zynq UltraScale+ MPSoC `https://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html`

2 Progress on Doctorate

2.1 Trenz-Serenity Adapter

Serenity[2], an ATCA blade with an industrial single board computer running Linux is the host for evaluating the possibility of using an heterogeneous device for all slow control tasks, an adapter to a commercial ZynqUS+ module has been designed. The Trenz to Serenity adapter, in its third revision, contains the addition of components like an on-board programmer based on the FTDI chip, a microSD card controller and includes bug fixes in the ethernet and usb physical interface chips. The adapter was utilized successfully to demonstrate the ability to boot two different programs in each of the processor types residing inside the system-on-module. The real-time capable R5 processors had the task to run an IPMC software from the company Pigeon Point while the application A53 processor were used to boot a Yocto/CentOS Linux distribution especially created for this application.

Figure 1: Trenz-Serenity adapter v1.3

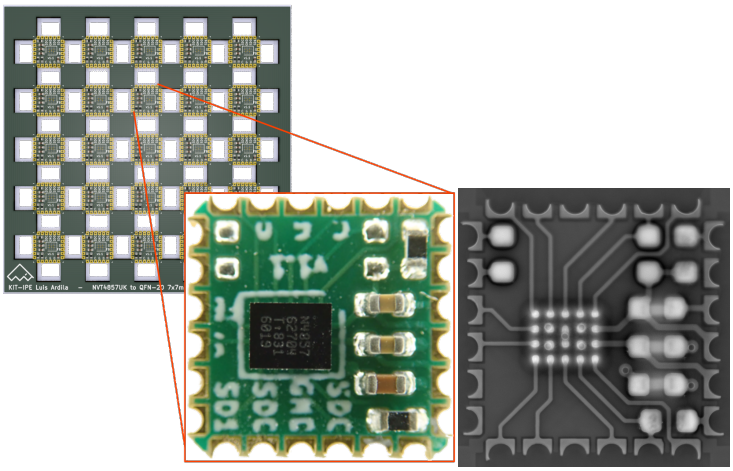
2.1.1 The microSD Card Controller

The microSD controller selected for the revision 3 of the Trenz-Serenity adapter supports the protocol SD3.0-SDR104 with up to 200 MHz of data transfer, the global electronics market driven by miniaturization in portable gadgets like cellphones has made that newer components supporting such high data rates protocols are only available in a very small package. The selected NVT4857UK SD-card controller chip has a Wafer Level Chip-Size Packages (WLCSP) with 0.4 mm pitch and 20 pins. This separation of the pins propose a big challenge to

[2]A. Rose and G. Iles, Serenity - An ATCA prototyping platform for CMS Phase-2, in TWEPP 2018 Topical Workshop on Electronics for Particle Physics, 2018.

fabrication houses and therefore the cost of producing a PCB board with those features rises significantly.

A two layer adapter was designed so that the complexity of the WLCSP package could be contained in a smaller PCB panel where fabrication issues could be monitor and controlled accordingly. The adapter contains 5 vias for breaking out the signals in the inner row of contacts, the vias were extended to be off-center with respect to the ball array so that the minimum distance between drills gets incremented as seen in Figure 2b, therefore avoiding costly via-in-pad technology and have a minimum separation between drills of 0.5 mm instead of 0.4 mm.



(a) Panel fabrication (b) X-Ray image

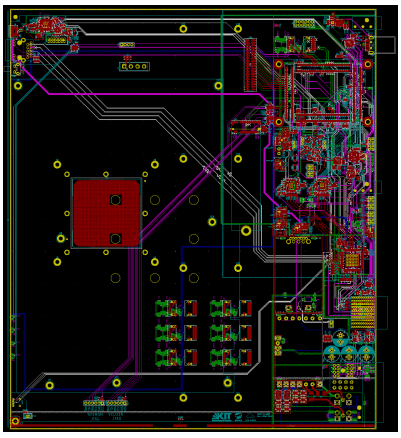
Figure 2: microSD controller module

In Figure 2a can be seen how the PCB design was done in a panel including 25 individual SD controllers, in this way, with a single fabrication one can produce several devices. Given the size of the component, some parameters had to be adjusted compared to the standard processing recipe at the assembly house. For instance, the thickness of the stencil used to print the solder paste is 100 μm instead of 120 μm, and it includes electro-polishing of the openings and nanoprotection of the surface to help in the lift-off process.

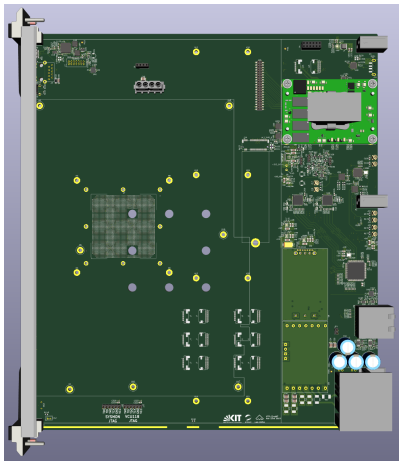
In Figure 2b an X-Ray image of an assembled microSD controller adapter is presented, it can be seen how the 20 pin ball array is optimally soldered with no bridges or mis-connections between the pads. from a 25 piece panel it was observed that only one had a solder bridge, it is necessary to perform optical inspection at each fabrication step to have traceability about the sources of errors and identify them effectively in the future.

2.2 ATCA ZynqMP Test Board

The use of a single device for performing IPMC communication via the back-plane to the shelf and general slow control based on CentOS Linux propose several power requirements which were not available when utilizing the Trenz to Serenity adapter. The ZynqMP ATCA board is designed to make the power up sequence available to the ZynqUS+ module and therefore be able to implement properly power isolation inside the SoC as well as control the power sequence accordingly.



(a) Design files with 12 layers for signal routing



(b) 3D render of the PCB

Figure 3: The ZynqMP ATCA Blade

The ATCA blade contains only the components required to perform slow control and IPMC, they are placed towards the back of the board, leaving the front accessible and unpopulated. Several mounting holes are provided in case the user wants to mount the VCU118 evaluation board from Xilinx. Two Samtec Firefly bidirectional high-speed links are available to interconnect the VU9P FPGA present in the evaluation board and the SoC in the Trenz module.

Two Ethernet links are available from the shelf in the back-plane connectors which are then connected to a central Ethernet switch with 7 ports. Two ports are dedicated to the SoC, one for the IPMC functionality and another for the Linux operating system. One port is routed to the front panel and it is available in a RJ45 connector. The blade provides an M.2 slot for mounting a SATA SSD and a USB OTG host port to connect any USB device like a keyboard or mouse, finally the board has a micro-USB port where the configuration cable is connected getting access to the JTAG and serial interfaces of the board. The Board has been fabricated and it is in the process of population of the components.

3 Publications

Posters and Proceedings

[1] L.E. Ardila-Perez, O. Sander, M. Balzer. "CMS R&D for Phase-2 Tracker Back-end Electronics". In: *System-on-Chip Workshop - CERN*. 2019. URL: https://indico.cern.ch/event/799275/contributions/3413734/attachments/1860874/3058571/SoC_RD_for_CMS_Phase-2_Tracker_Back-end_Electronics.pdf.

[2] L.E. Ardila-Perez, O. Sander, T. Schuh, D. Tcherniakhovski, D. Bormann, M. Balzer, M. Weber. "EureKA-Maru: an ATCA board for the CMS Phase 2 Tracker Upgrade with centralized slow control and board management solution based on a Zynq Ultrascale+ System-on-Chip". In: *Topical Workshop on Electronics for Particle Physics TWEEP2019*. 2019. URL: https://indico.cern.ch/event/799025/contributions/3486510/.

[3] O. Sander, L. Ardila-Perez, D. Tcherniakhovski, M. Balzer, M. Weber. "A novel centralized slow control and board management solution for ATCA blades based on the Zynq Ultrascale System-on-Chip". In: *24th International Conference on Computing in High Energy & Nuclear Physics CHEP2019*. 2019. URL: https://indico.cern.ch/event/773049/contributions/3474311/attachments/1933805/3211730/CHEP19_ZUSP_IPMC.pdf.

[4] Andrew Rose, Duncan Parker, Gregory Iles, Ozgur Sahin, Pierre-Anne Bausson, Andromachi Tsirou, Giacomo Fedi, Pierro-Giorgio Verdini, Luis Ardila, Matthias Balzer, Thomas Schuh, Tom Williams, Alessandro Thea, Kristian Harder, Shashi Dugad, Raghunandan Shukla, and Irfan Mirza. "Serenity: An ATCA prototyping platform for CMS Phase-2". In: May 2019, p. 115. DOI: 10.22323/1.343.0115.