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CMS Level 1 Track Trigger

An FPGA Approach

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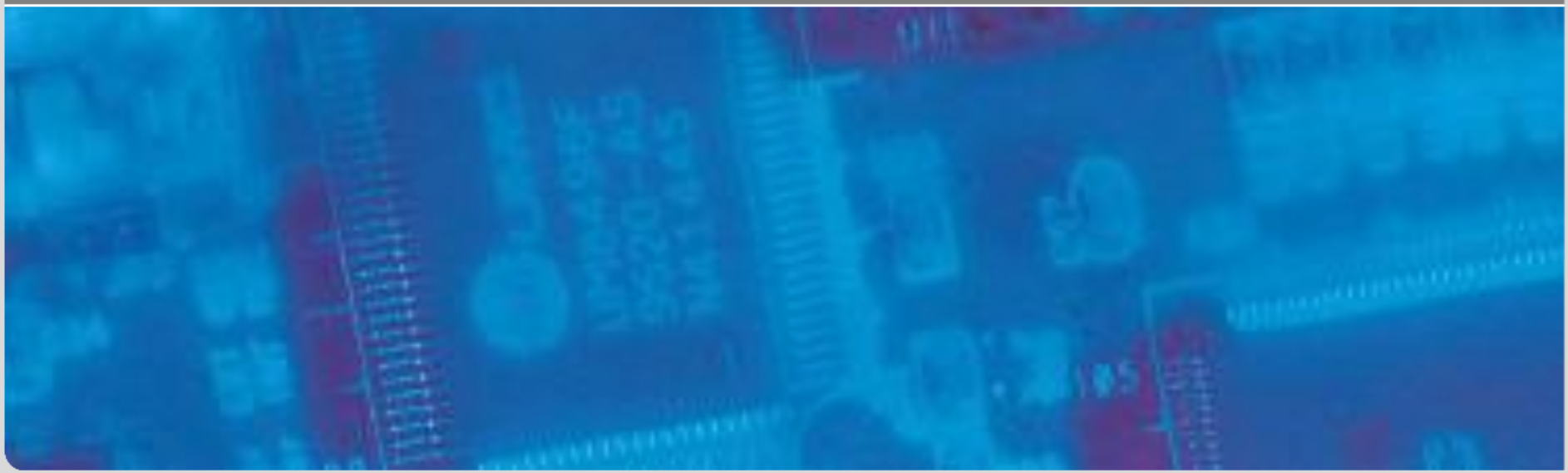
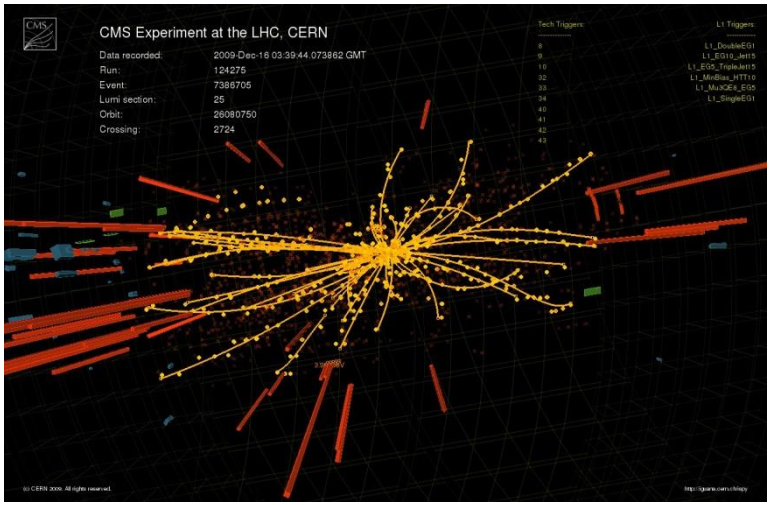
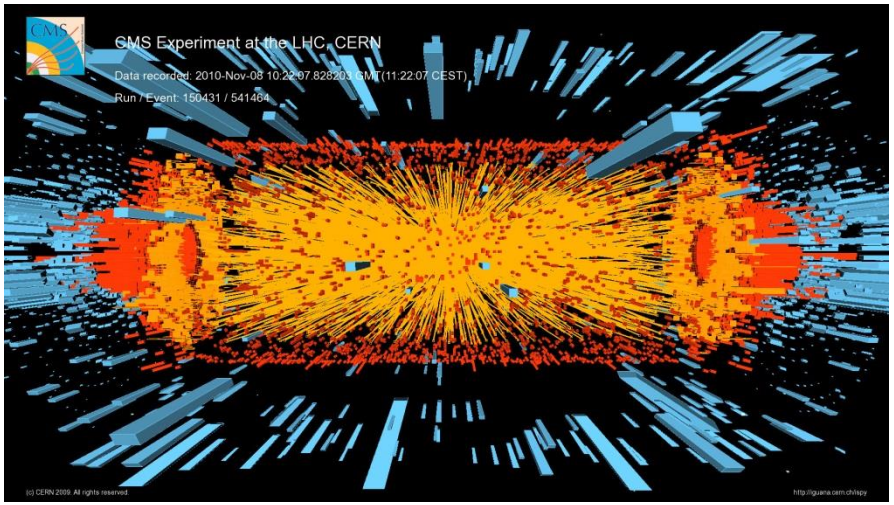


Motivation: LHC Upgrade Phase 2

LHC today

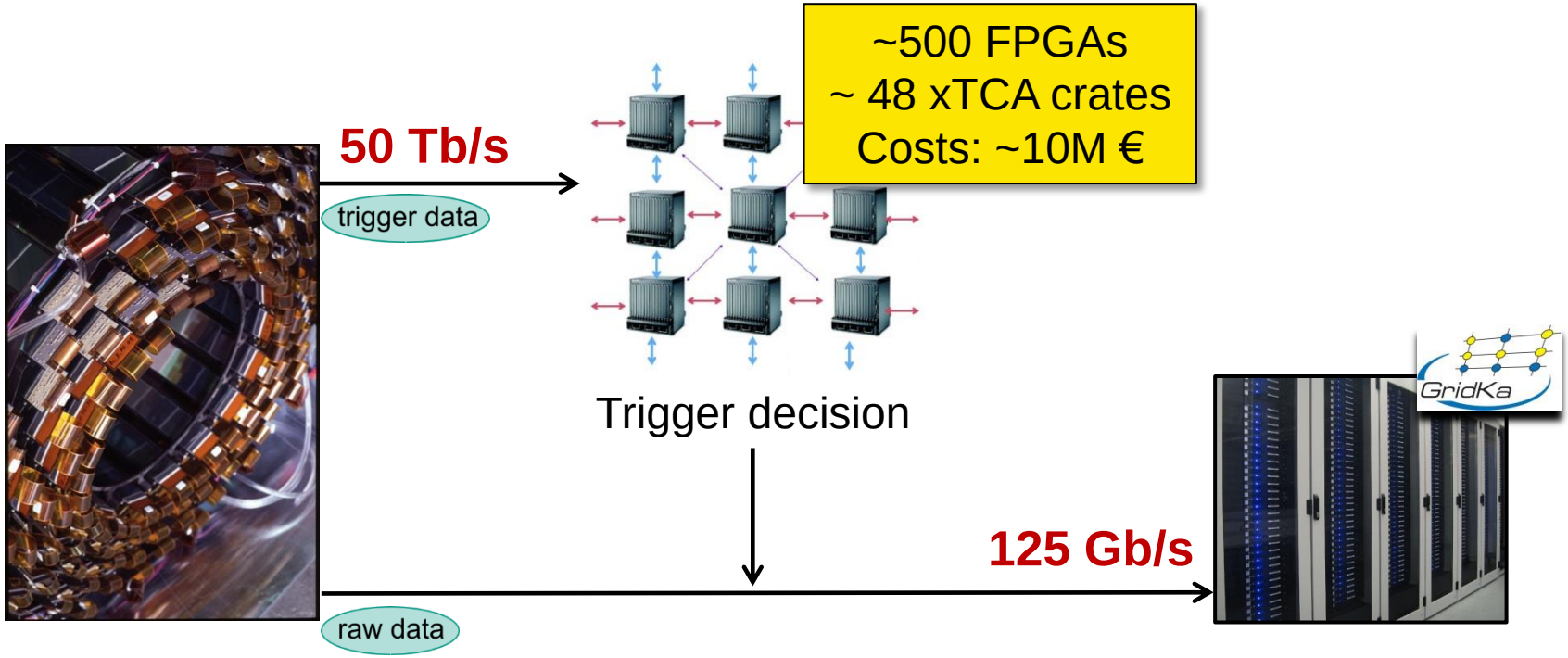


HL-HLC ~ 2023



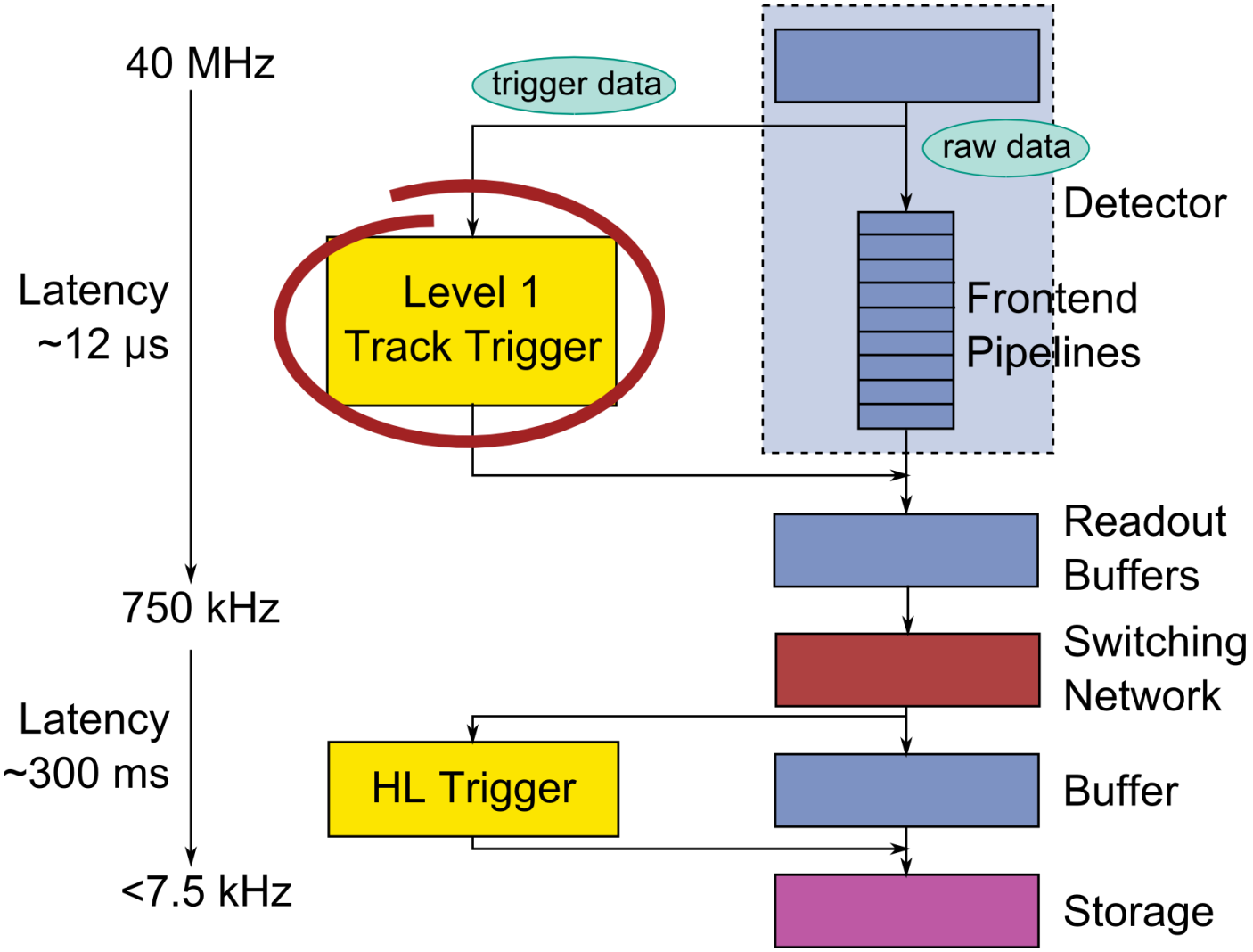
- Increasing luminosity by a factor of 10
- Input data rate ~ 100 Tb/s

CMS Experiment - Challenges

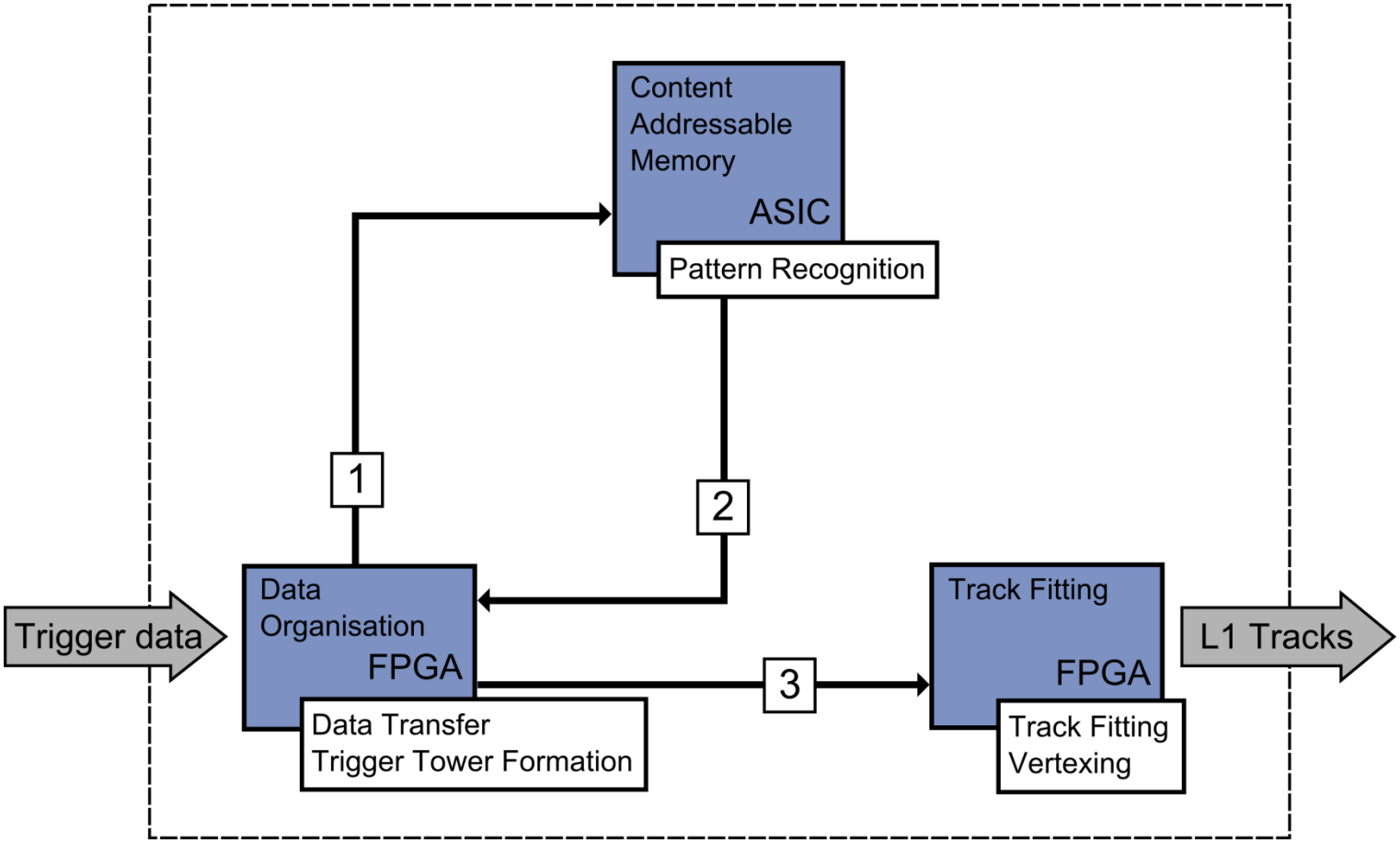


- Reduce data by factor 400 (online)
- Trigger decision latency ~ 12 µs

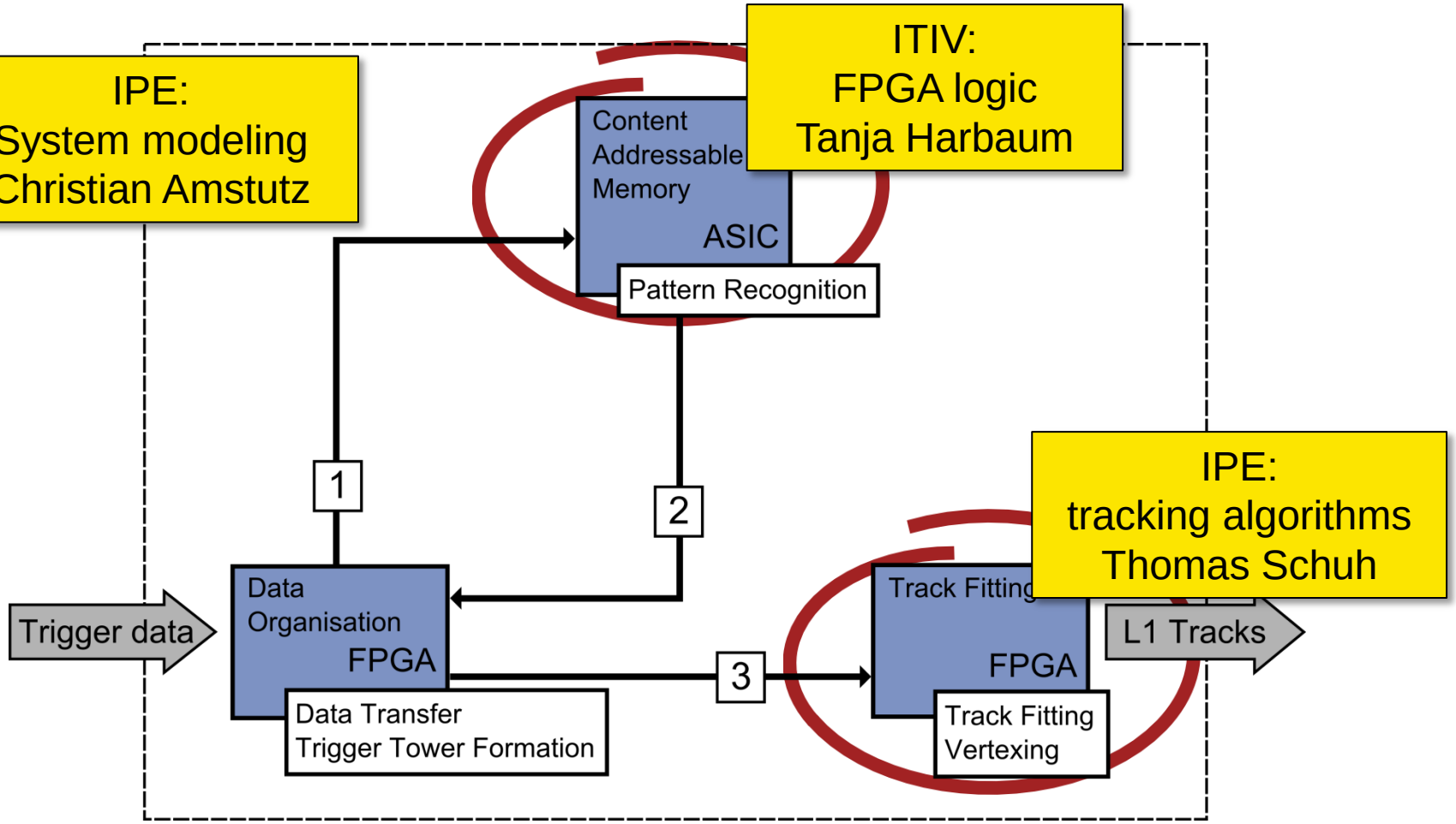
CMS Trigger System



Current Level 1 Track Trigger Board

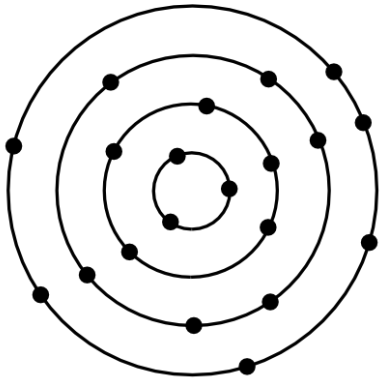


Current Level 1 Track Trigger Board

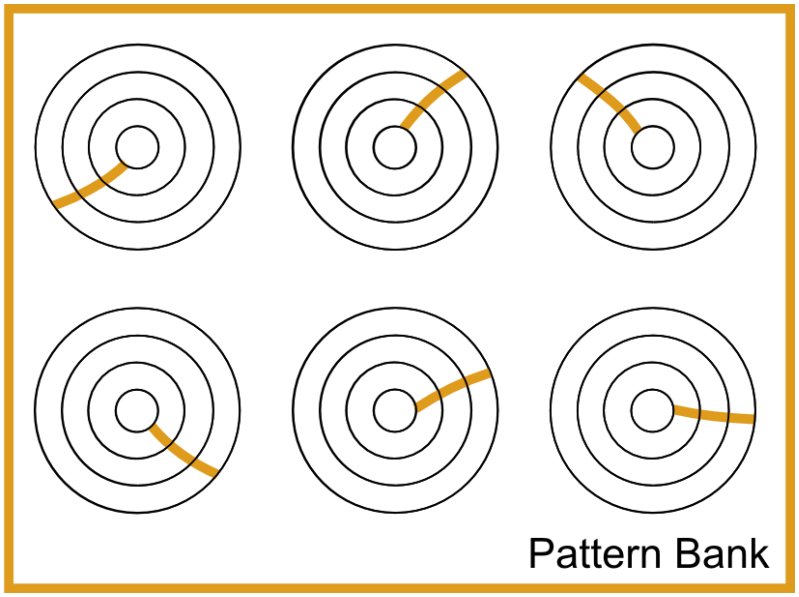


- Instead of 1 AM-ASIC and 2 FPGAs, might also choose 2 FPGAs or 1 big FPGA?

Pattern Recognition - Idea

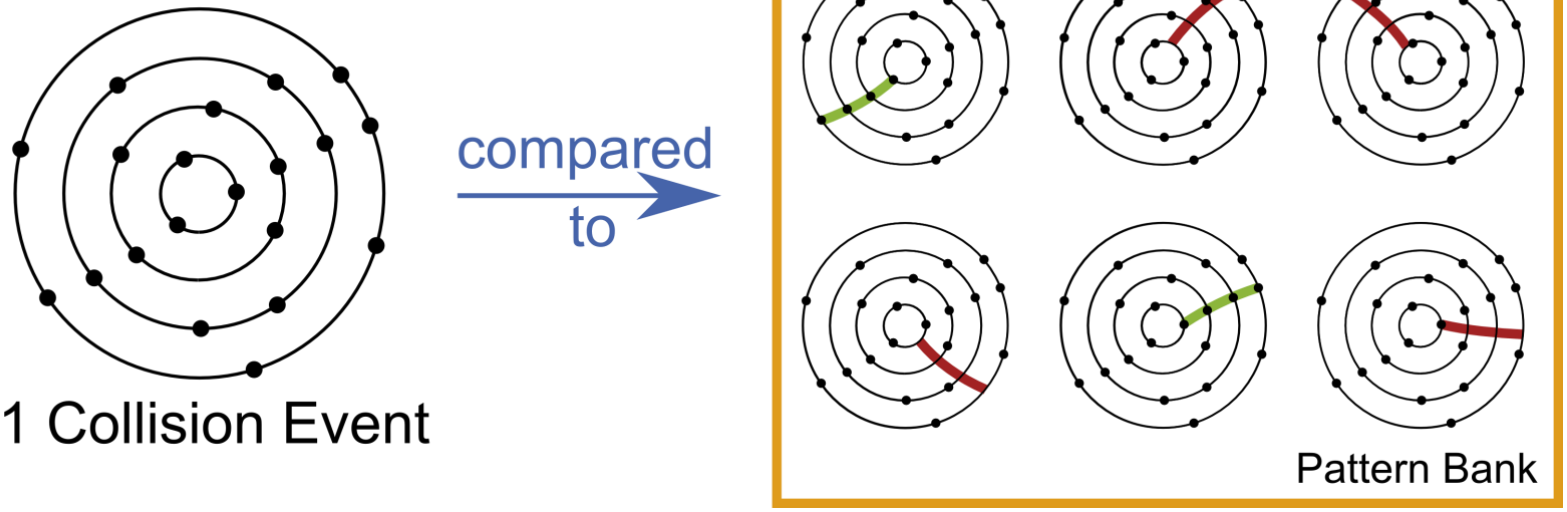


L1 Collision Event



We know what interesting particles look like!

Pattern Recognition - Idea



We know what interesting particles look like!

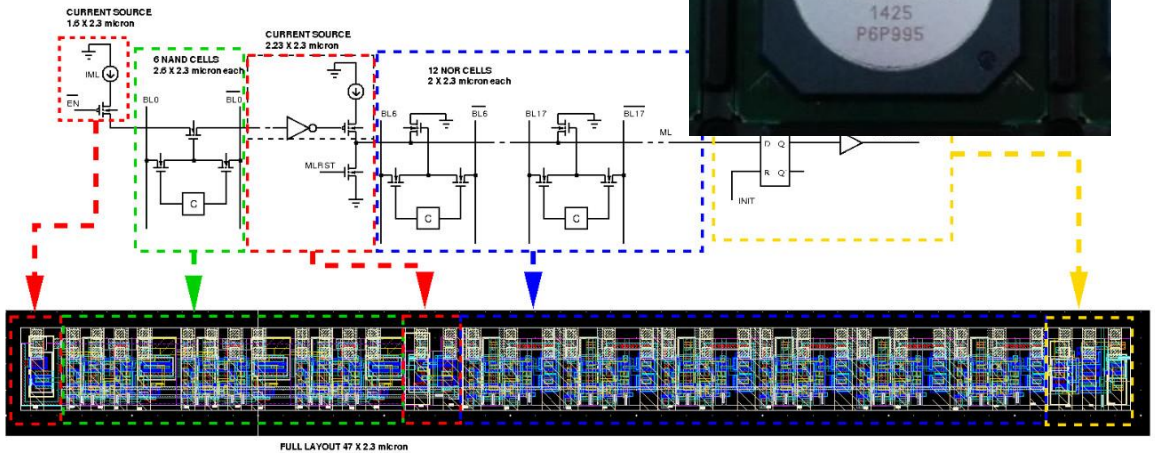
Application-Specific Integrated Circuit (ASIC)

- Integrated Circuit (IC) customized for a particular use

\+ Fast and efficient

— Cost of development > 1M €

— Design time > 2 years

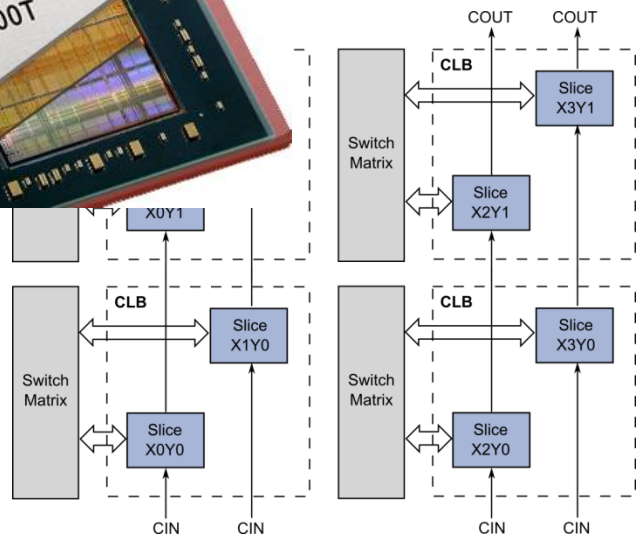


Field-Programmable Gate Array (FPGA)

- Commercial IC programmed by customer
- Configurable logic blocks (CLB) includes lookup tables (LUT)

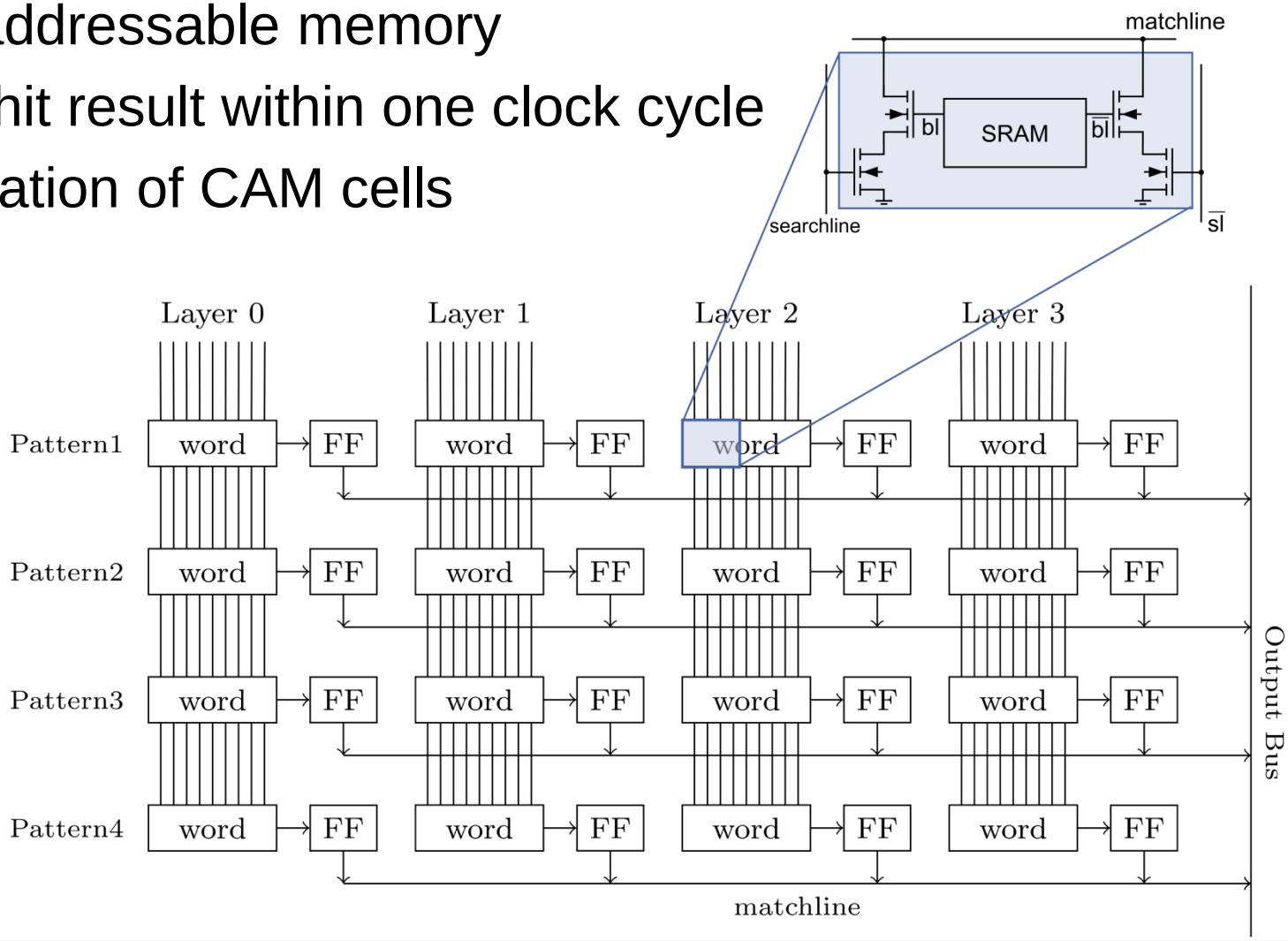
\+ Short implementation period
\+ Reconfigurable

— Reduced clock speed
— Power consumption
— Logic density



Pattern Recognition – AM Chip

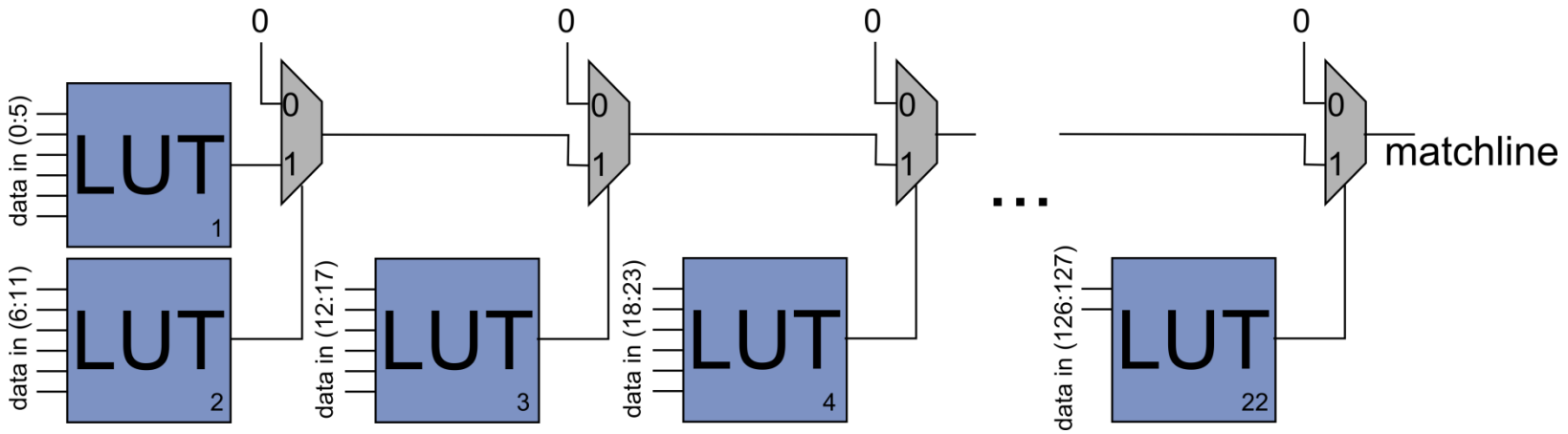
- Content-addressable memory
- Provides hit result within one clock cycle
- Concatenation of CAM cells



Pattern Bank

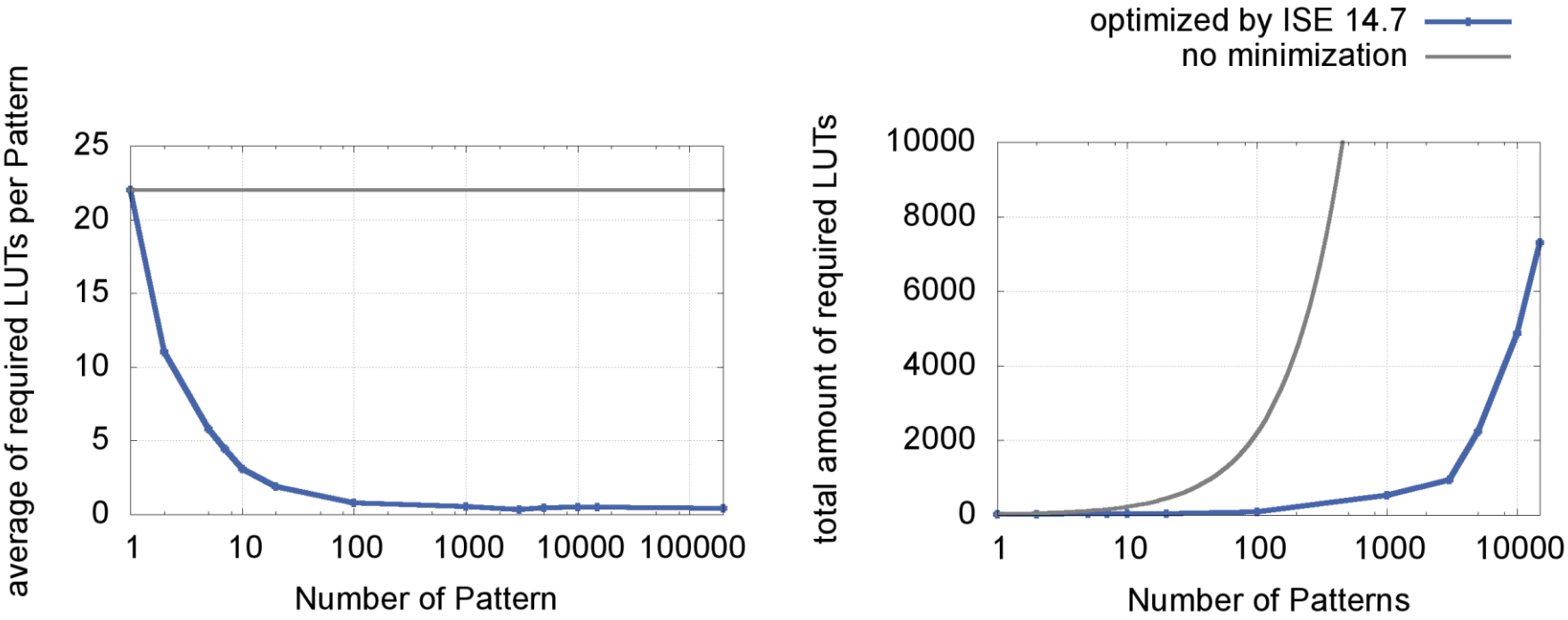
Layer 0	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5	Layer 6	Layer 7
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000100	0100010000101001	0000010000010111
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000100	0100011100011000	0100000100000001
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000000011	0000100010000101
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000010001	0000100010000101
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000010001	0000100010000111
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000010001	0000110010000111
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000010001	0000110010000011
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000010001	0000110010000101
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000010001	0000110010000011
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000110	0000100000010001	0000110010000101
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000101	0000100000010000	0000110010000011
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000101	0000100000010000	0000110000010000
0000000000000000	0000000000000000	0000000100000100	0000001111000000	0000011110000000	0001000100000101	0000100000010000	0000110010000011
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000010000	1000010000101000	0000110010000001
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000010000	1000010000101000	0000110000000100
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000010000	1000010000101000	0000110010000011
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000010000	1000010000101000	0000110010000101
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000110000	1000010000101000	0000110000000010
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000110000	1000010000101000	0000110000000100
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110000000100
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110000000110
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110010000101
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110010000111
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000100000000000
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000100000000010
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000100010000001
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110000000110
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110010000101
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110010000111
0000000000000000	0000000000000000	0000000101000001	0000001111000000	0000011110000000	0100000000100000	1000010000101000	0000110000000100

FPGA Approach – Minimization by Logic



- LUT structure for one pattern
  - 22 LUTs
  - Pure combinatorial logic – no clock cycle
  - Plus one 128 bit register to store the input

FPGA Approach – First Results



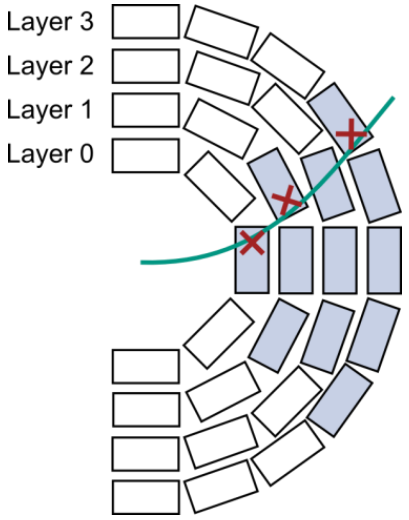
- Gain saturates – 0.5 LUT per pattern in average
- Depends on the composition of the Pattern Bank

➡ Extensive minimization by logic is possible

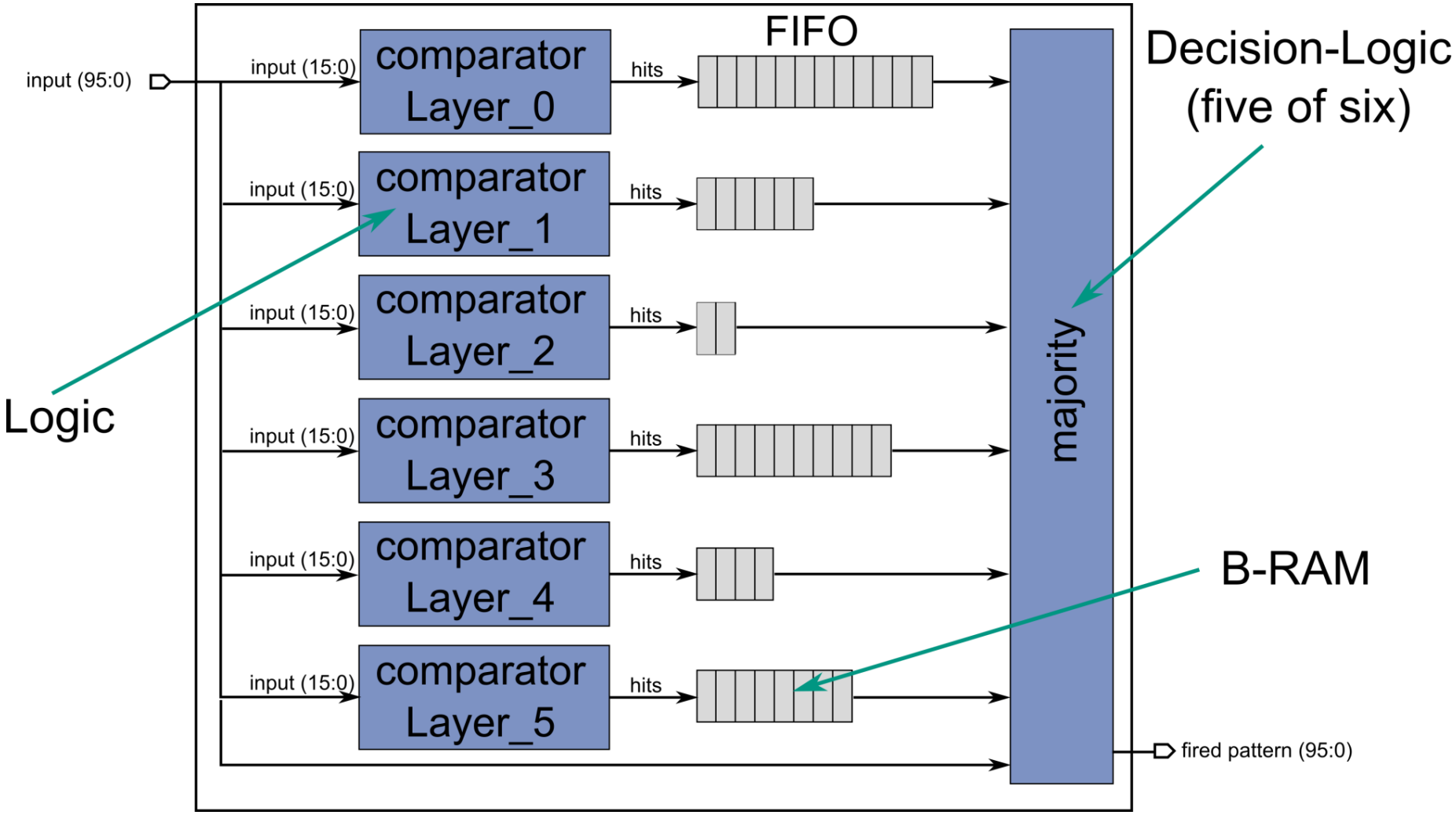
Comparison with AM-Chip

- AM-Chip offers additional features
- Writeable memory
  - ➡ Synthesize the FPGA

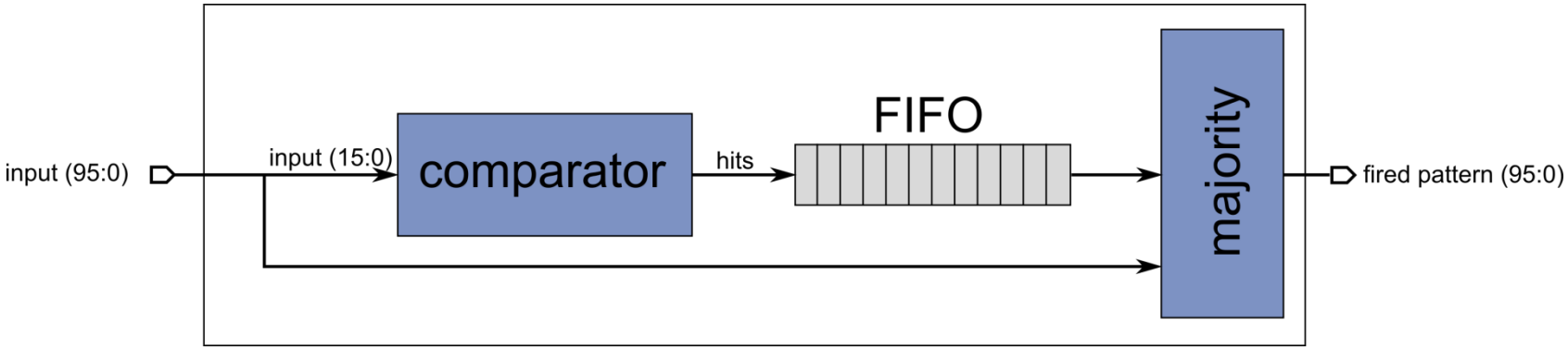
- Handle failure layers
  - ➡ Split pattern into layers (96 Bits → 6*16 Bits)
    - Duplicate pattern
    - Layer-based approach



Layer Based Approach

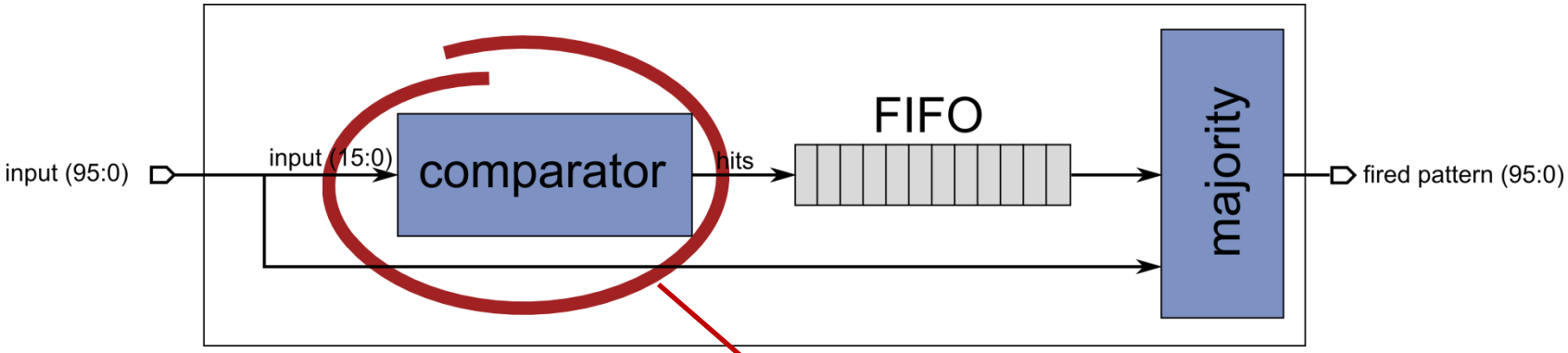


Layer Based Approach – one layer



- Comparator
  - Input: 16 Bits
  - Output: n Bits fired pattern number
- FIFO
  - Buffers fired Pattern
- Majority Matrix
  - Decision (five of six, four of six, …)

Layer Based Approach – Comparator

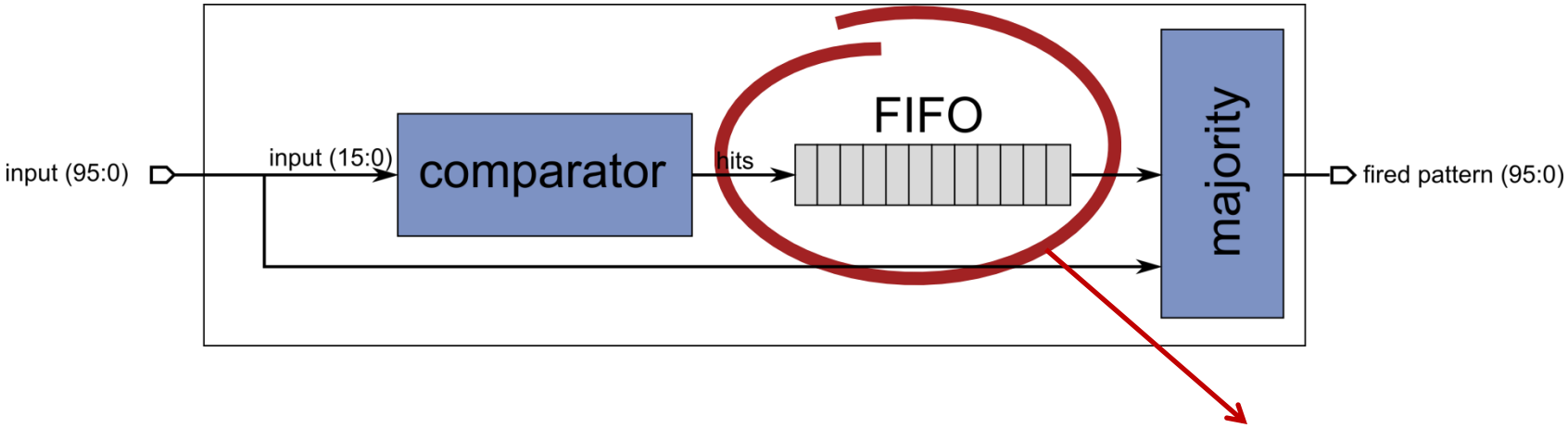


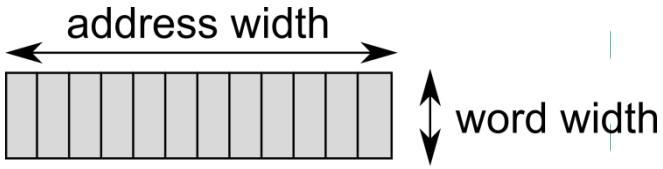
- Pure logic (state machine)
  - Pre-computed
  - Depends on stored pattern
- Use only Lookup tables
- Minimize by vendor tools

```
if (input="00100000010000111") then
    hit0<="00000000";
end if;

if (input="000110001000001") then
    hit0<=" 00000001";
    hit1<=" 10001001";
    hit2<=" 10100011";
end if;
```

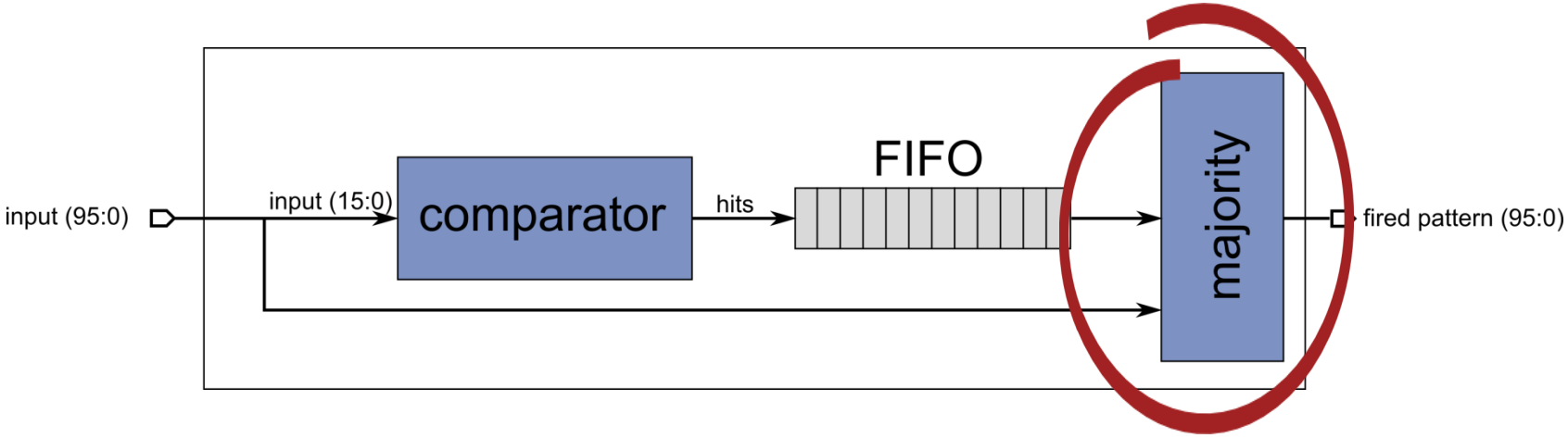
Layer Based Approach – FIFO





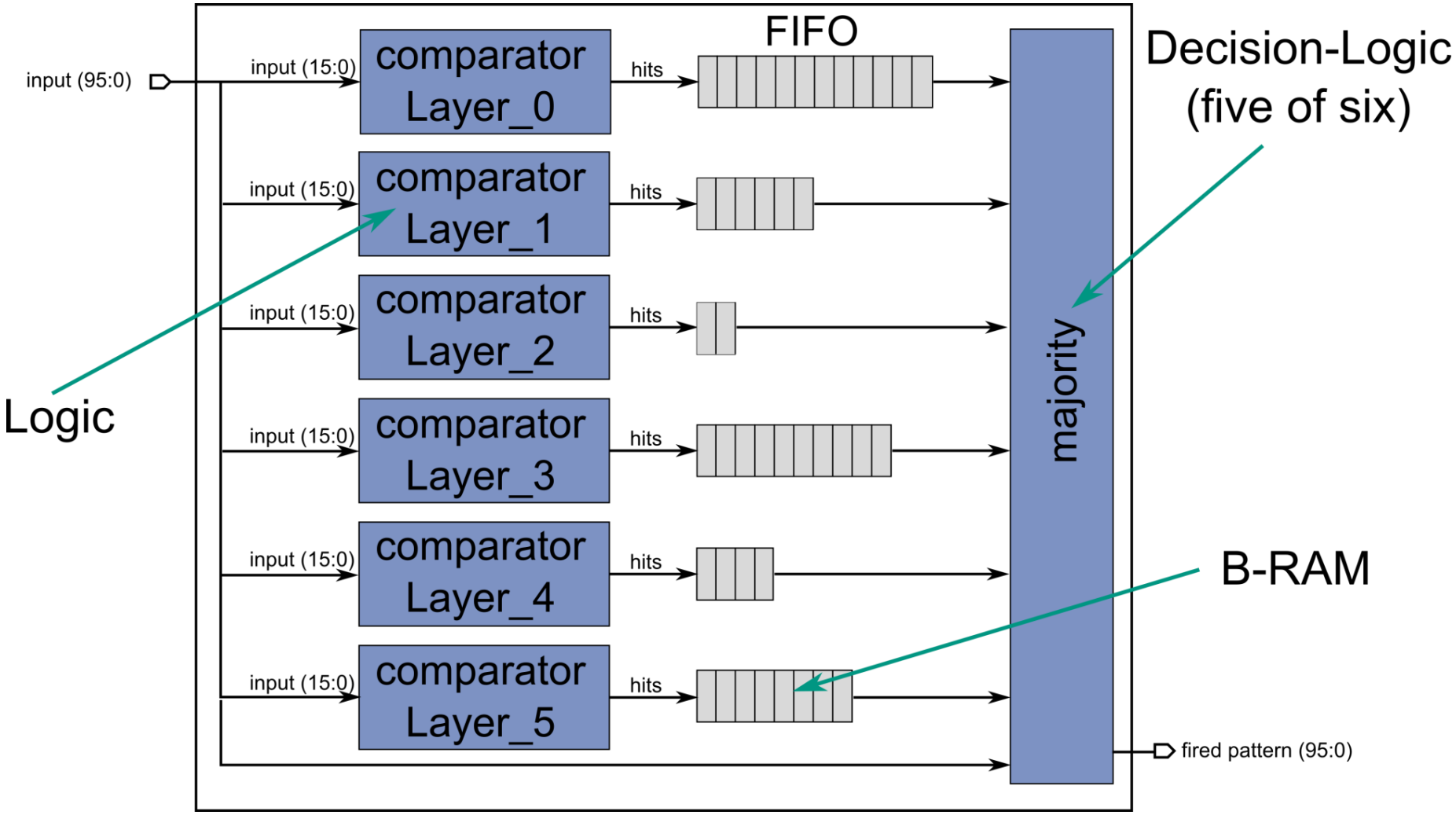
- Buffer
- Use block RAM
- Variable size
  - Address width <= $\log_2$ (number of max possible hits)
  - Word width <= $\log_2$ (number of stored pattern)

Layer Based Approach – Majority Unit



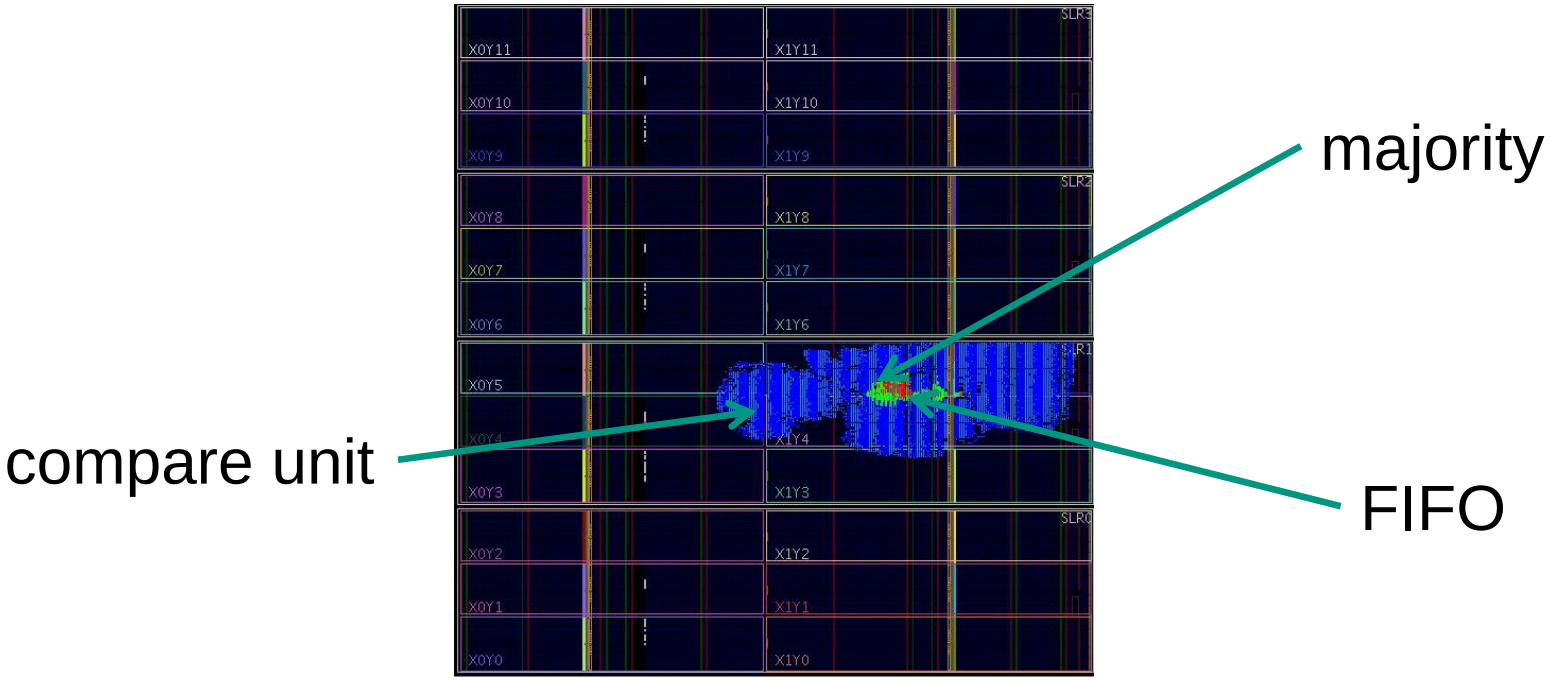
- Selection of fired pattern
  - Pure logic

Layer Based Approach



Layer Based Approach – First Results

- Design for 10k pattern is running
  - 180MHz clock cycle
  - 26 FIFOs with max 400 entries
  - <10% Utilization of an huge up-to-date FPGA



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Thank you for your attention.

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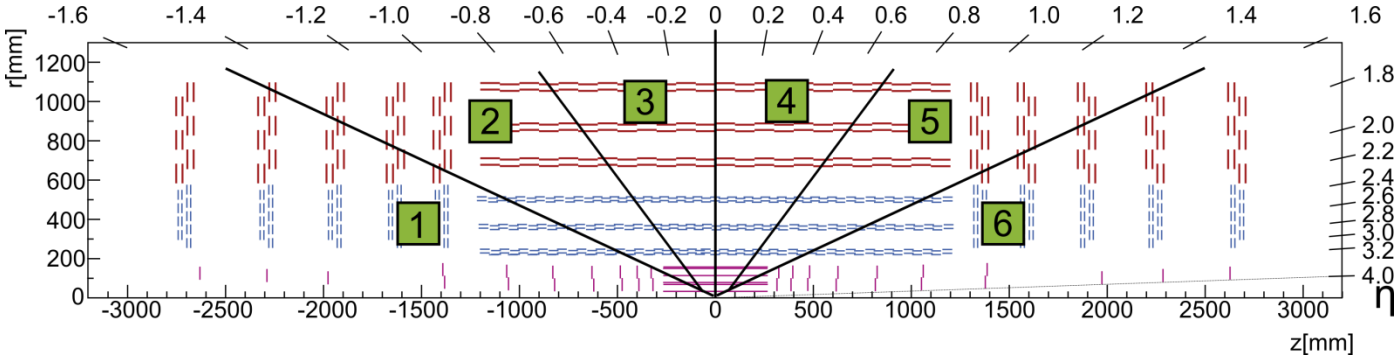
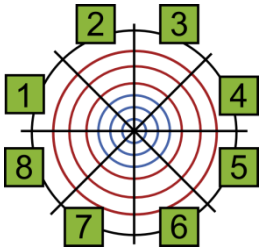
BACKUP SLIDES

CMS Detector – 48 Trigger Towers

- 6 Sectors (r-η)Plane X 8 Sectors (r-ϕ)Plane

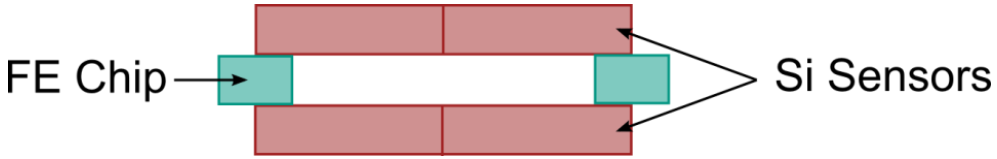




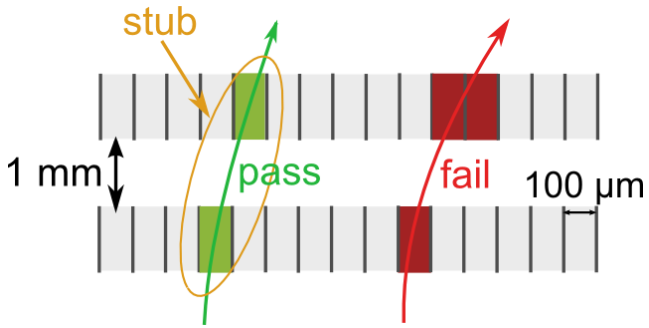
- 48 trigger sections
  - 200 Stubs per Event in average
  - Up to 500 Stubs per Event possible
  - 400 – 600 Gb/s per Trigger Tower
- 50 Tb/s Amount of L1 Data
  - ~15.000 Fibers (Modules) each 3.25 Gb/s

CMS Detector – Outer Tracker Modules

- p_T Module Concept

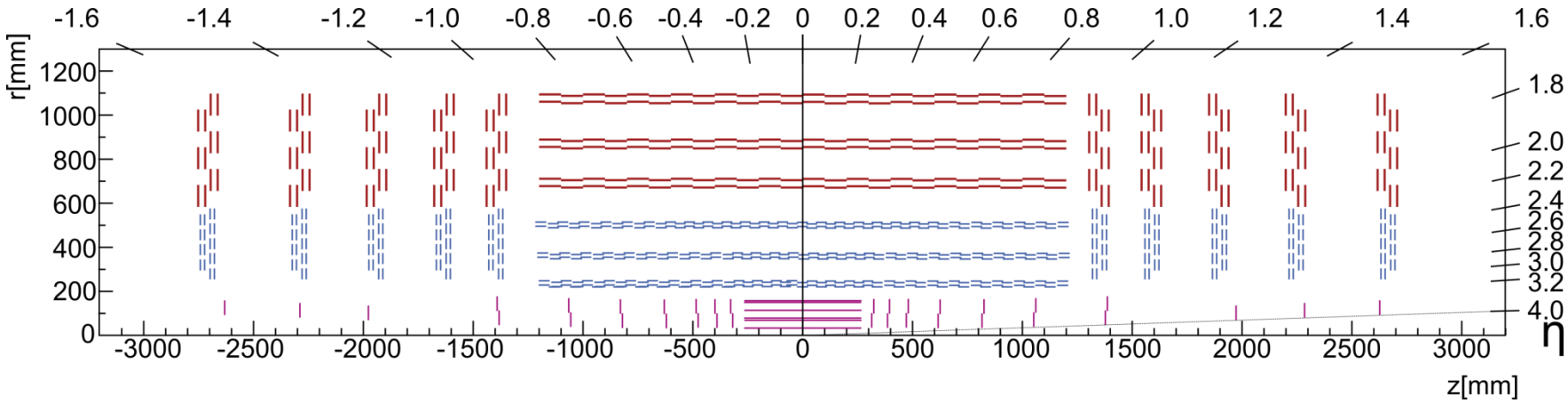


- Stub – Pair of Clusters in the two Sensors



➡ First rough p_T Cut at the Module Level

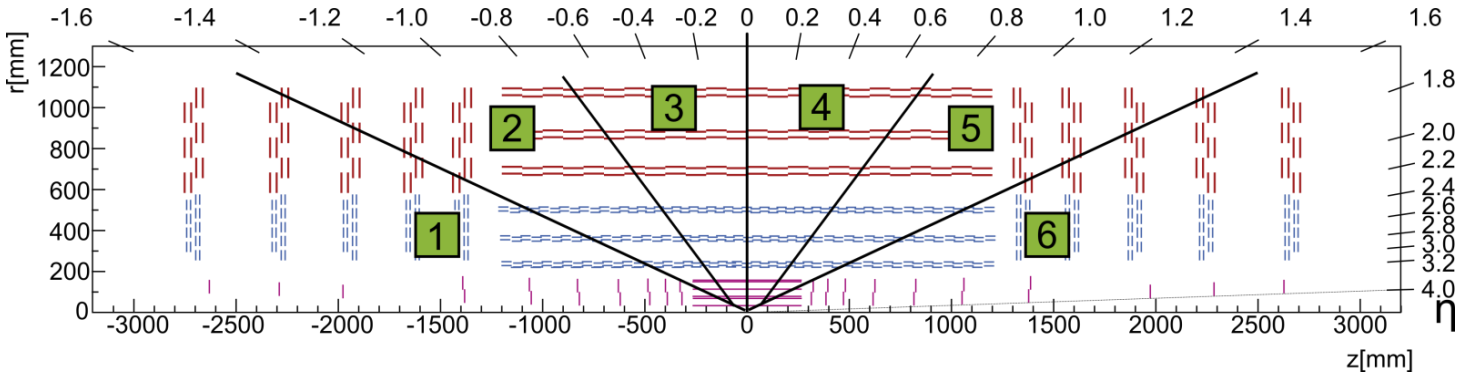
CMS Detector - Barrel-Endcaps Geometry

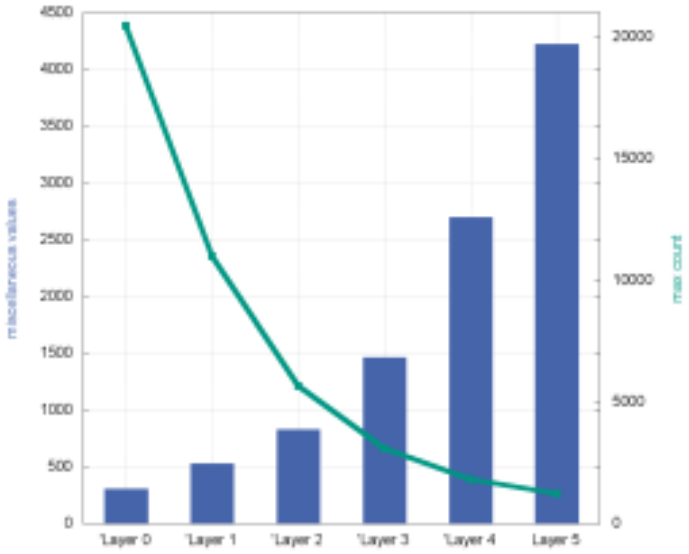


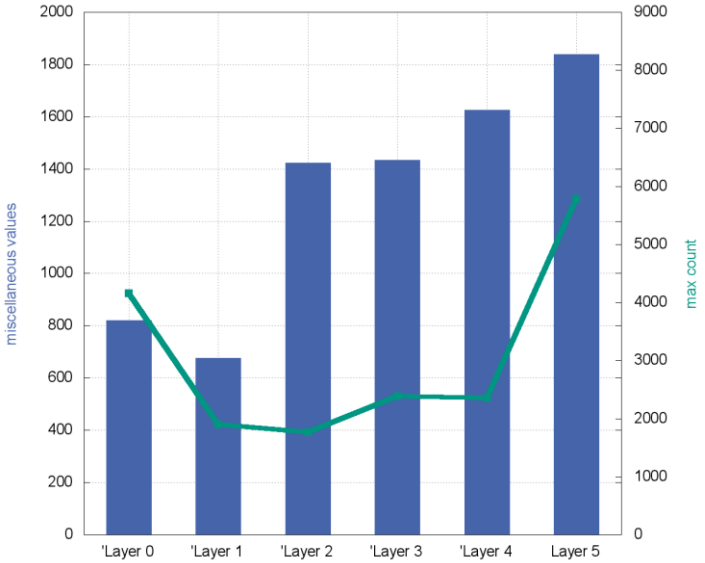
- Inner Pixel
  - 4 BPIX + 10 FBIX
- Outer Tracker
  - 7084 PS Modules (1 macro-Pixel + 1 Strip Sensor)
  - 8424 2S Modules (2 Strip Sensors)

Part used at L1

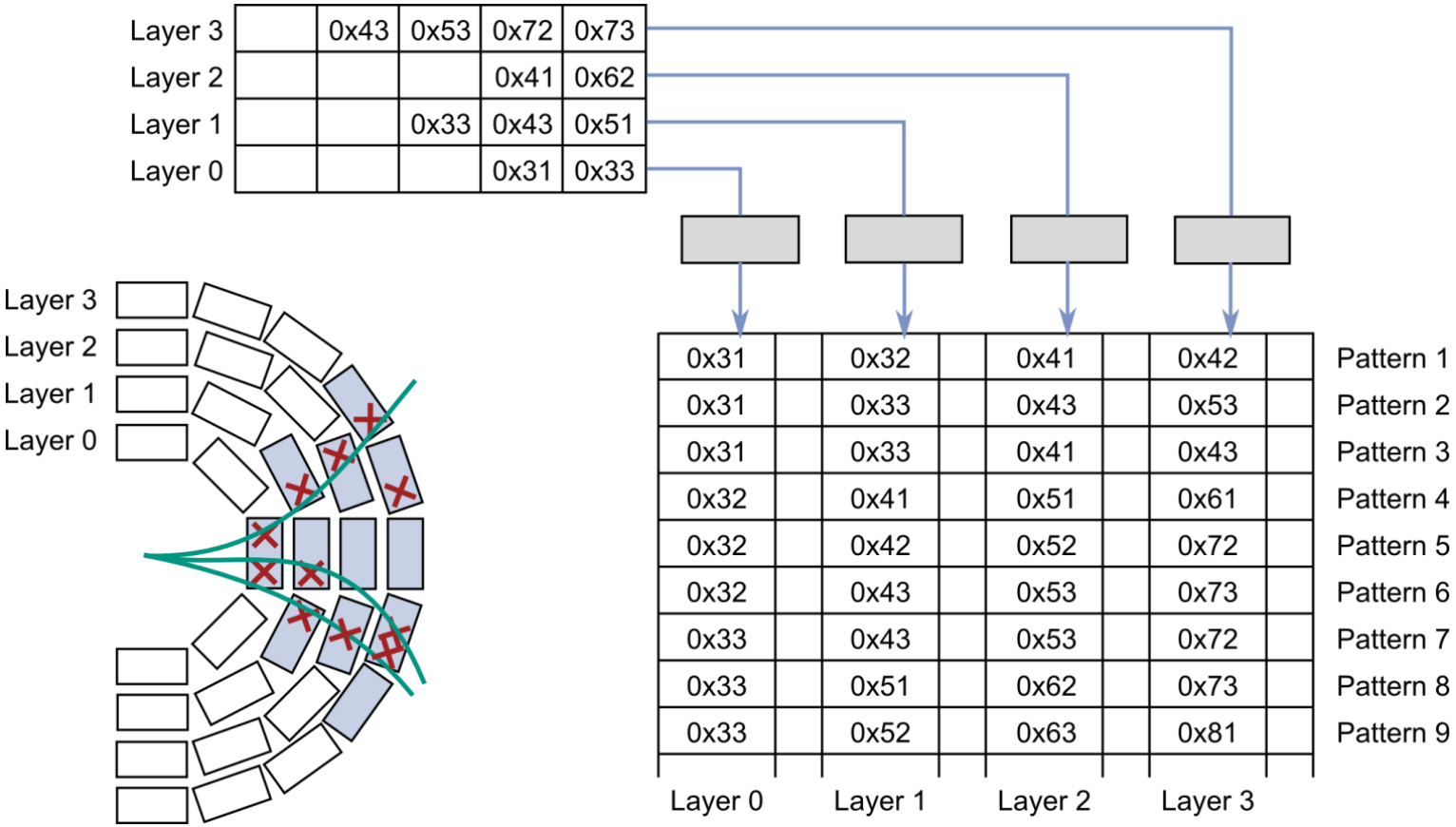
Analyzed Pattern Bank - First Results



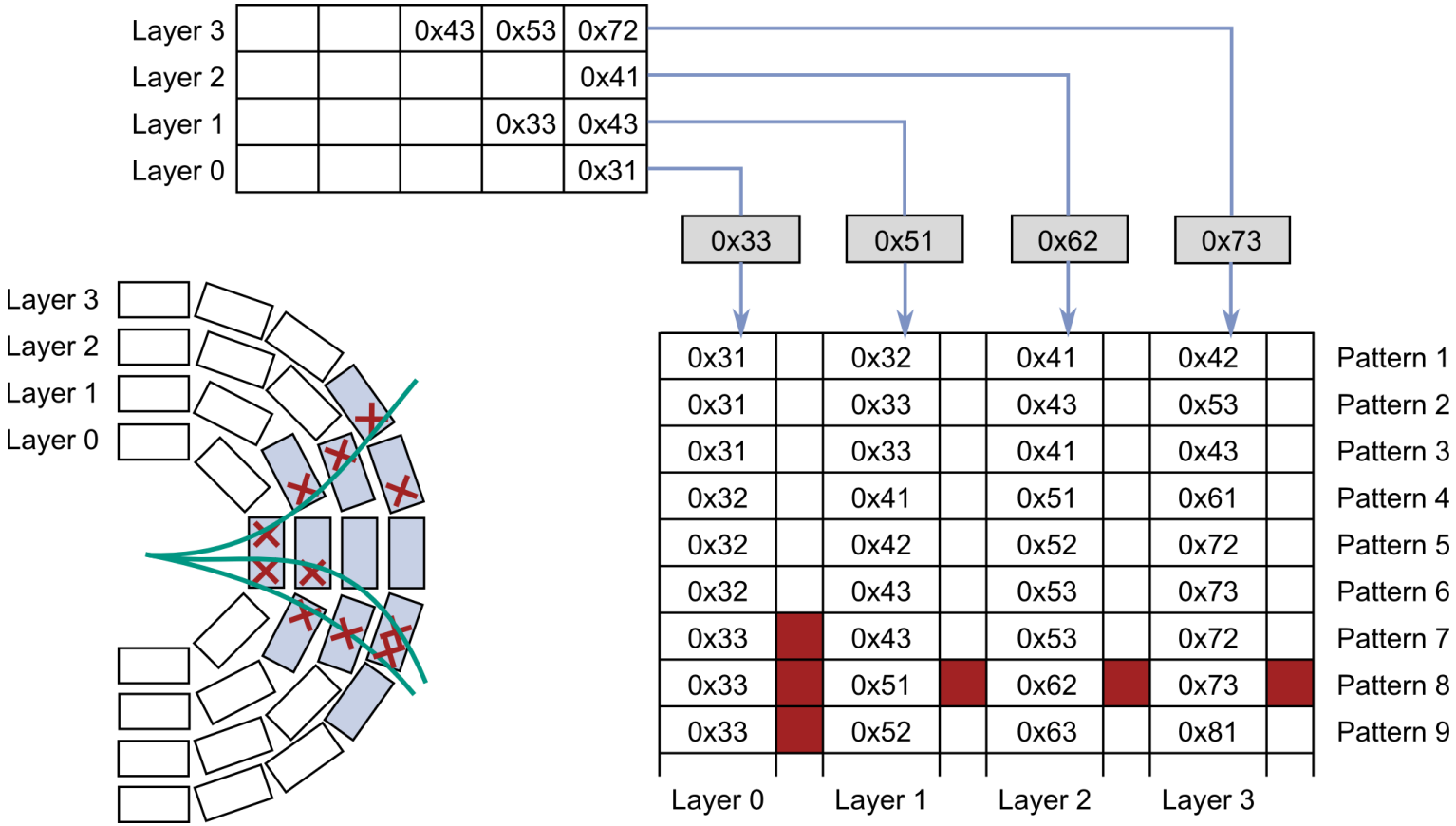




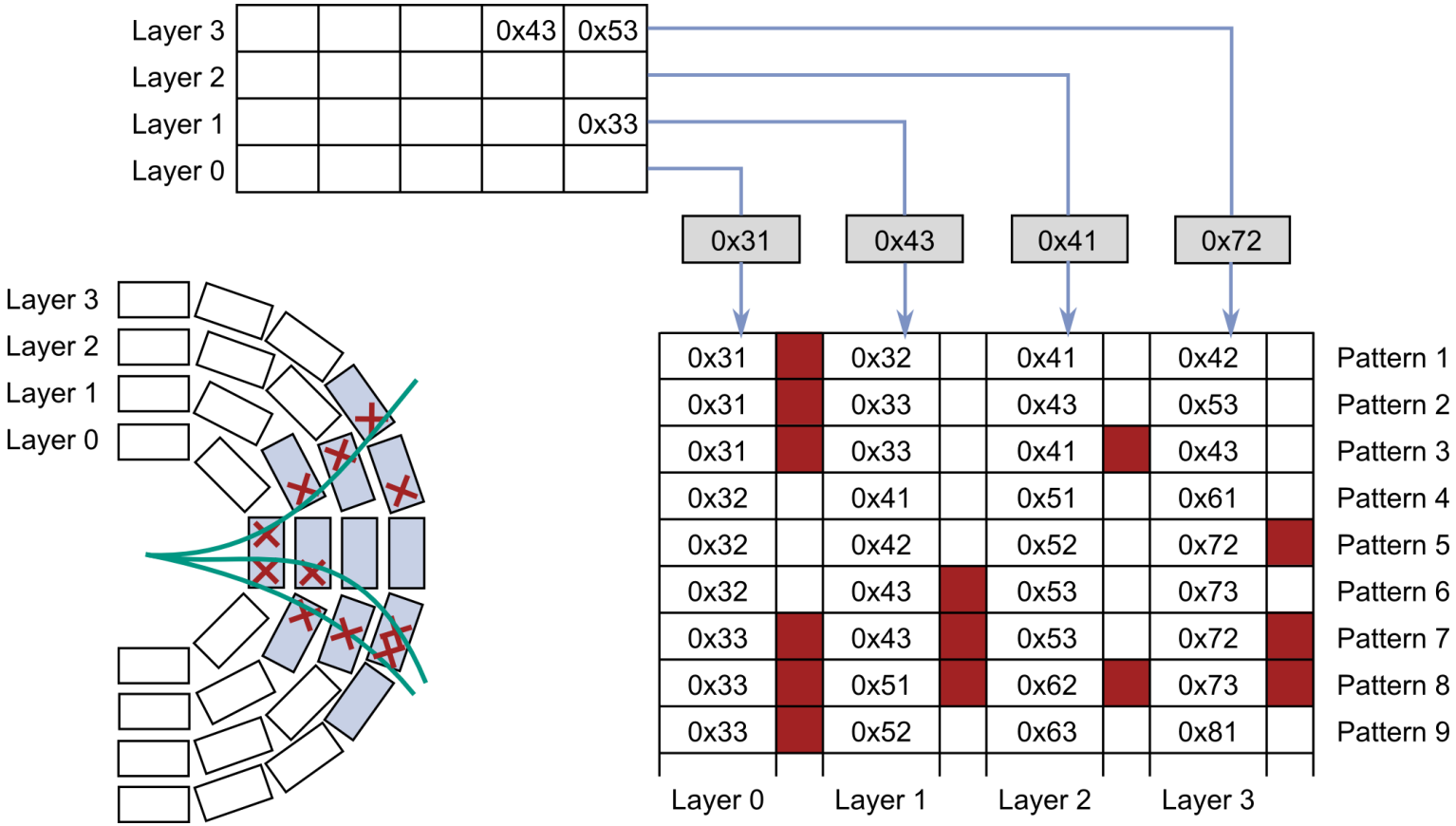
AM Chip – Operating Mode



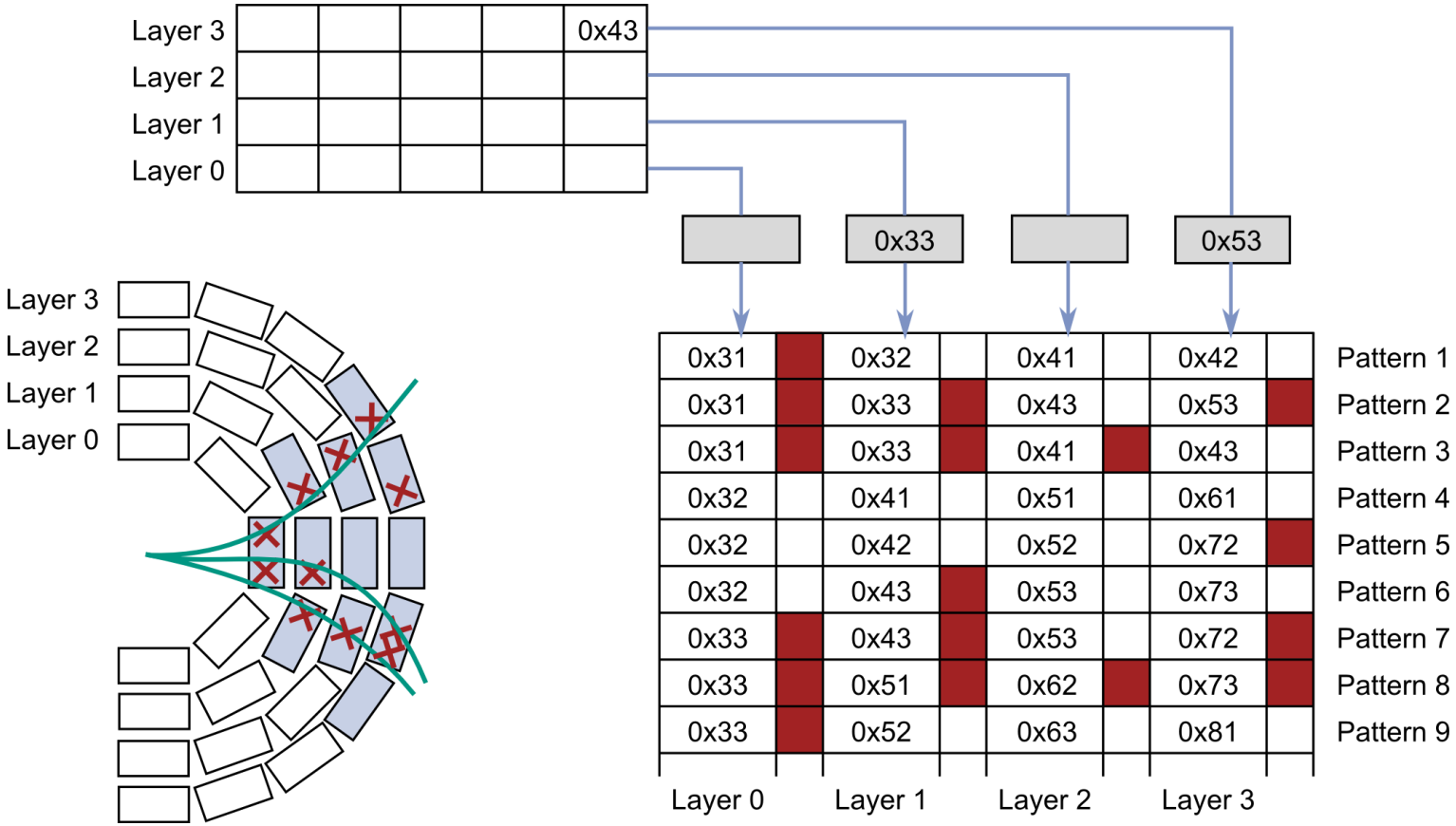
AM Chip – Operating Mode



AM Chip – Operating Mode



AM Chip – Operating Mode



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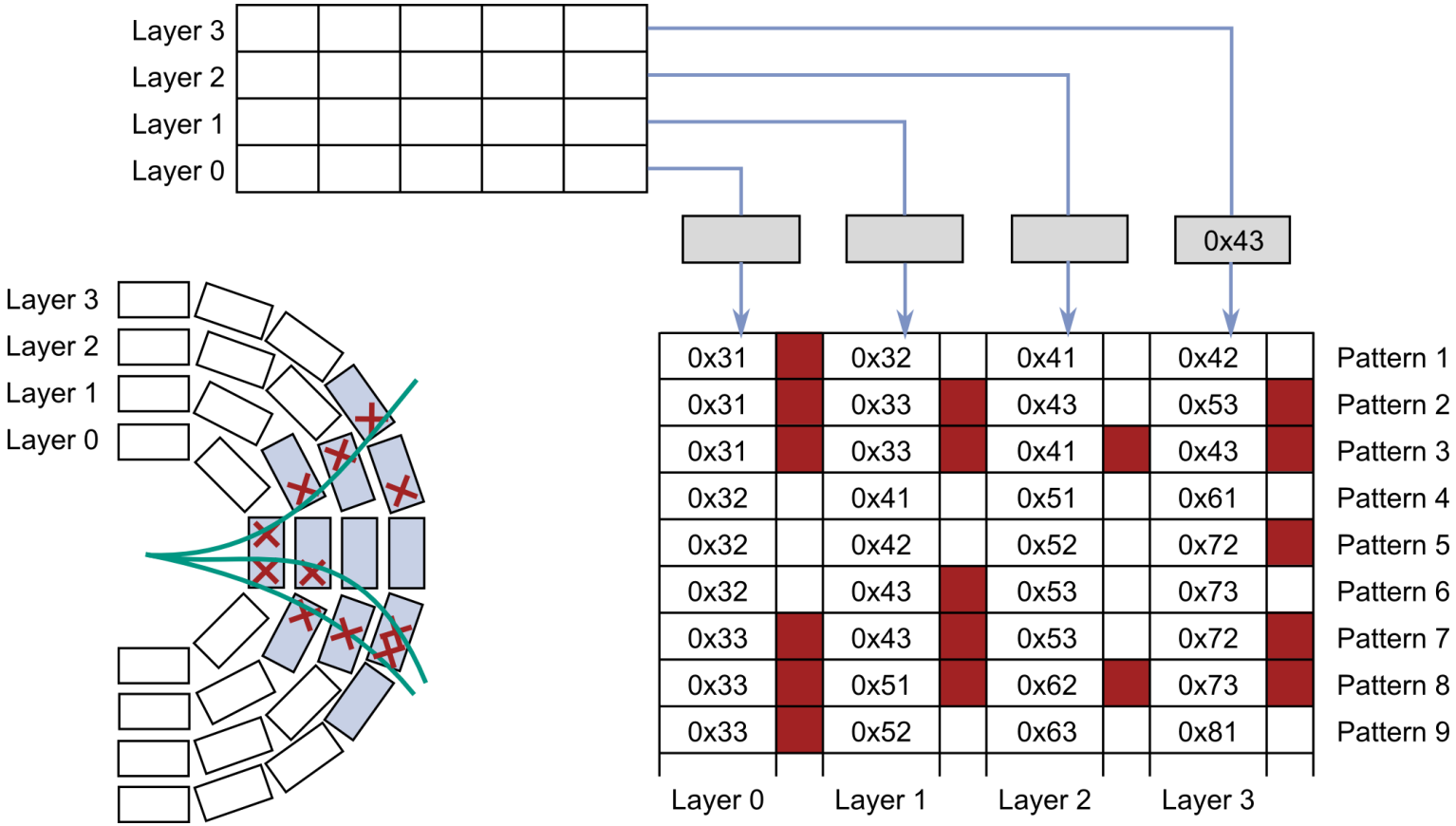

AM Chip – Operating Mode