

KSETA Report 2020

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Project Description

As I started in May, I was given two tasks to work on. One was to build a data acquisition (DAQ) hardware for a satellite demonstrator, that is used to test the features for the Tandem-L satellites.

The Tandem-L demonstrator system consists of three Modules each controlled by a Kintex Ultrascale FPGA. Two of these modules are the so called DRPUs (digital receiving and processing units). They each feature 16 ADC channels that sample the input signal at 2.6 GHz. For the highest accuracy, they need to be synchronized as good as possible.

The data acquisition (DAQ) module houses eight ADCs that can translate the signal from the intermediate frequency of 1257,5 MHz to the baseband.

To enable the best synchronization, a symmetric clock tree is necessary. A symmetric clock tree equals all deterministic delays out. This way, only stochastic delays take effect on the cross channel skew. These result from length mismatches and delays within ICs. All in all the resulting delay adds up to 200 ps. It is therefore three magnitudes lower than the demanded maximum 190 ns.

Besides the 8 ADCs and the corresponding clock tree, the DAQ-modules contain Firefly-Connectors that interconnect the two modules and connect to a third one, the storage-module. This storage-module is also controlled by the same FPGA as the DAQ-Modules and its purpose is to save the processed data onto SSDs. By end of 2020, the schematics were handed over for layout.

The second project I was given is to expand the functionality of the platform management that controls the CMS Track-Trigger (Serenity) board. This platform is developed for high-throughput (up to 10 TBit/s) general-purpose data-processing.

In present, an x86-based ComExpress-Module communicates with the platform via an FPGA that is used as port-expander. The platform communicates with the ATCA shelf manager via an IPMC-Module. The aim was to combine these three actors into a single Zynq SoC.

Therefore a demonstration needs to be done, in order to show this concept is feasible. My task is to adapt the software from the x86-module to a Zynq-

ARM-module that is replacing it. By the end of 2020 the PCIe-link between the SoC and the port-expander is to be established. Once a stable link exists, the software is ported to ARM.

Activities within KSETA

none