

KSETA Report 2021

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Project Description

Tandem-L

In year 2021, the Tandem-L project continued. It started with the Layout being developed as well as the schematics for the second board being expanded and finished.

As the Tandem-L board is similar to the ECHO-DAQ board, the lessons learned there could be implemented during layout. So the power supply planes for the highly noise-sensitive clock chips had to be moved from underneath the switched-mode power supplies to another place. Also the linear regulators of the clock chips were replaced with ones that have a higher power supply noise rejection ratio.

Afterwards the PCB and the components were ordered and composed for assembly. As not all components arrived before the end of the year, the board could not be assembled in 2021.

CMS

The project that was mainly worked on is the Serenity-A board which is developed for the CMS experiment. An in-house Zynq Multi-Processor (ZynqMP)-powered mezzanine module should be explored as an option to the x86-based ComExpress module that was used on Serenity-Z. For that, an AXI Chip2Chip-connection has been established between the ZynqMP and the Virtex Ultracale+ FPGA that is on board of the Serenity-A board.

On the Serenity-A's Virtex Ultrascale+ FPGA, the EMP-framework is instantiated. It provides a standardized in- and output for the algorithms that are then used on the board. This framework is controlled by the board-management module using an IPBus connection. This IPBus-connection needs to be carried over the AXI Chip2Chip link, so the link has been integrated into the EMP-framework. Since any EMP projects are built using the code-based IPBus builder (IPBB), the AXI Chip2Chip is generated within the builder using a tcl-script.

Besides that, another part of firmware was ported to the ZynqMP, namely the Serenity Management Shell (SMASH). SMASH performs the slow-control of the board like setting up clocks, enabling power supplies or reading the status of the firefly transmitters and receivers. On the Serenity-Z from Imperial College, SMASH controls an Artix FPGA that is connected to the ComExpress module via PCIe. As the Artix is not present on the Serenity-A, the logic is instead instantiated inside the ZynqMP's programmable logic. Using also the IPBus protocol, parts of the work for the EMP-framework could be reused here.

In late 2021, a hardware rework of the Serenity-A board was performed in which some end-of-life components have been replaced and the clock-distribution has been reworked to support synchronous and asynchronous clocks instead of only asynchronous ones. As the I2C connections in the Serenity-A were causing some troubles, a completely new I2C bus architecture has been established for the new version. Finally, the highest speed firefly transmitters need a higher input voltage that is now also generated and can be selected using a jumper.

Activities within KSETA

- System-On-Chip Laboratory (Analog part)
- Statistical methods in particle physics data analysis
- Introduction to astroparticle physics
- Organic Semi-conductors
- OLED-displays: From fundamental solid state physics to a multi-billion € industry
- Broad introduction into modern experimental particle physics